TB-FMCH-HDMI2
Hardware User Manual
1 IN/OUT + Audio support

Rev.1.00

Revision History

Version	Date	Description	Publisher
Rev.1.00	2011/03/29	Initial release	Yoshioka

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Introduction

Thank you for purchasing the **TB-FMCH-HDMI2－RX/TB-FMCH-HDMI2-TX** boards. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
	Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
	Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is HDMI interface for Xilinx FPGA evaluation boards. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Board Accessories

All documents relating to this board can be downloaded from our website Club-X.

Accessories:

Interboard spacers and screws

Interboard jumper cable

2. Overview

The TB-FMCH-HDMI2 comes either with AnalogDevices's HDMI Receiver "ADV7612BSWZ-P" or HDMI Transmitter "ADV7511KSTZ-P".

(Collectively, there are called TB-FMCH-HDMI2. This document specifically describes these optional boards in the RX and TX sections respectively).

Each board has two independent receivers/transmitters and is designed for high resolution support.

It uses Samtec's FMC connector and Molex's HDMI connector for connection with a platform board having High-Pin Count connectors.

This User Manual is refer to 1 channel input/output and audio(I2S format) support ROM files.

TB-FMCH-HDMI2 boards need to download following ROM files.

Table 2-1 ROM data

No	Board name	FPGA ROM data
1	TB-FMCH-HDMI2-RX	tb_fmch_hdmi2_rx_1ch_audio_100.mcs
2	TB-FMCH-HDMI2-TX	tb_fmch_hdmi2_tx_1ch_audio_100.mcs

3. Feature

HDMI Devices

Receiver : AnalogDevices's ADV7612BSWZ-P

Transmitter : AnalogDevices's ADV7511KSTZ-P

FMC Connector : Samtec's ASP-134488-01

HDMI Connector (common) : Molex's 5002541927

Power Supply (common) : Jumper switch selection

The RX board has an EEPROM for Display Data Channel (hereafter referred to as DDC) and allows setting the AnalogDevices's ADV7612BSWZ-P board operation via jumpers.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 3-1 FMC Connector Pin Layout

4. TB-FMCH-HDMI2-RX

4.1. Block Diagram

Figure 4-1 shows the TB-FMCH-HDMI2-RX block diagram.

The FMC-HPC connector is mounted on the solder side of the board.

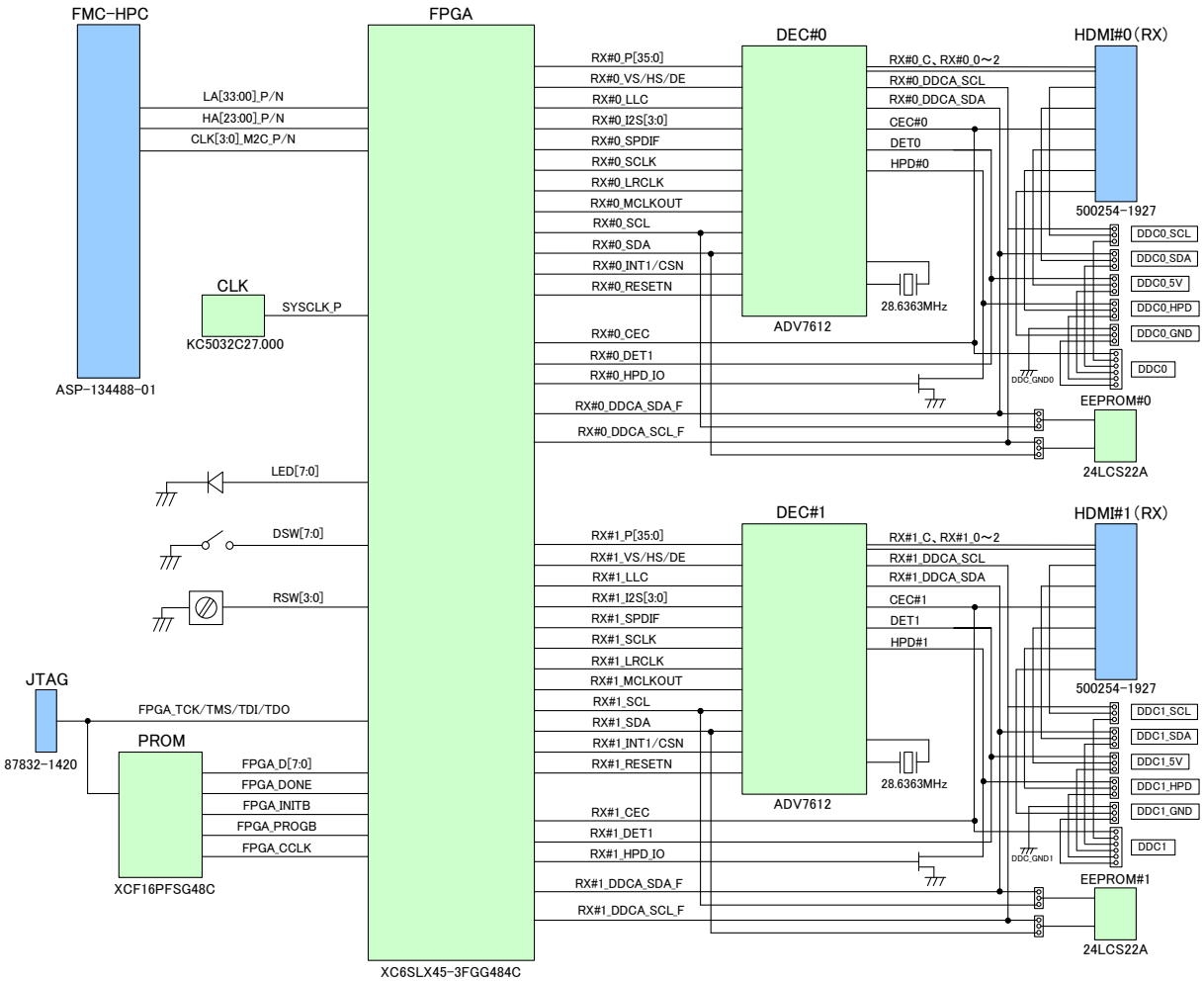

Figure 4-1 TB-FMCH-HDMI2-RX Block Diagram

Main Functions:

1. HDMI receive function (ADV7612 => FPGA)
2. FMC connector interface (FPGA => FMC-HPC connector)
3. EEPROM interface
4. JTAG interface
5. General-purpose clock interface (27MHz)
6. General-purpose switch
7. General-purpose LED
8. DDC connection (Normal/ Through)

Note: This design uses HDMI#0(RX) only. Because of limited pin number of FMC-LPC.

4.2. External View of the Board

Figures 4-2 and 4-3 show the external view of the TB-FMCH-HDMI2-RX board.

Caution : This board has a plastic cover for protecting HDMI devices. Do not remove a plastic cover.

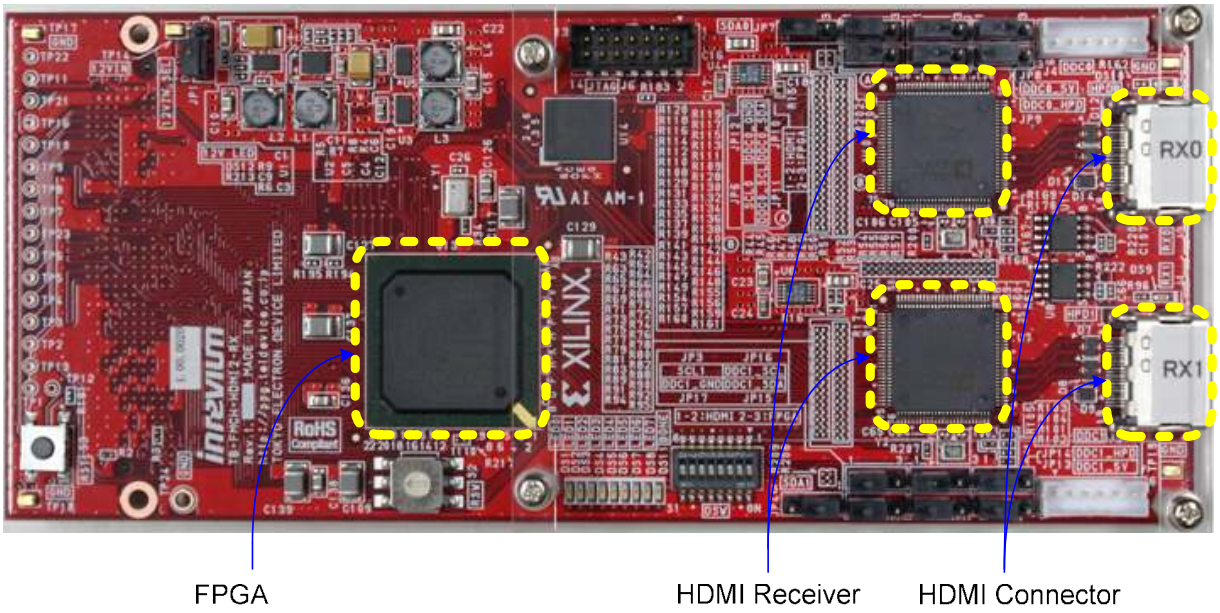

Figure 4-2 External View of TB-FMCH-HDMI2-RX (component side)

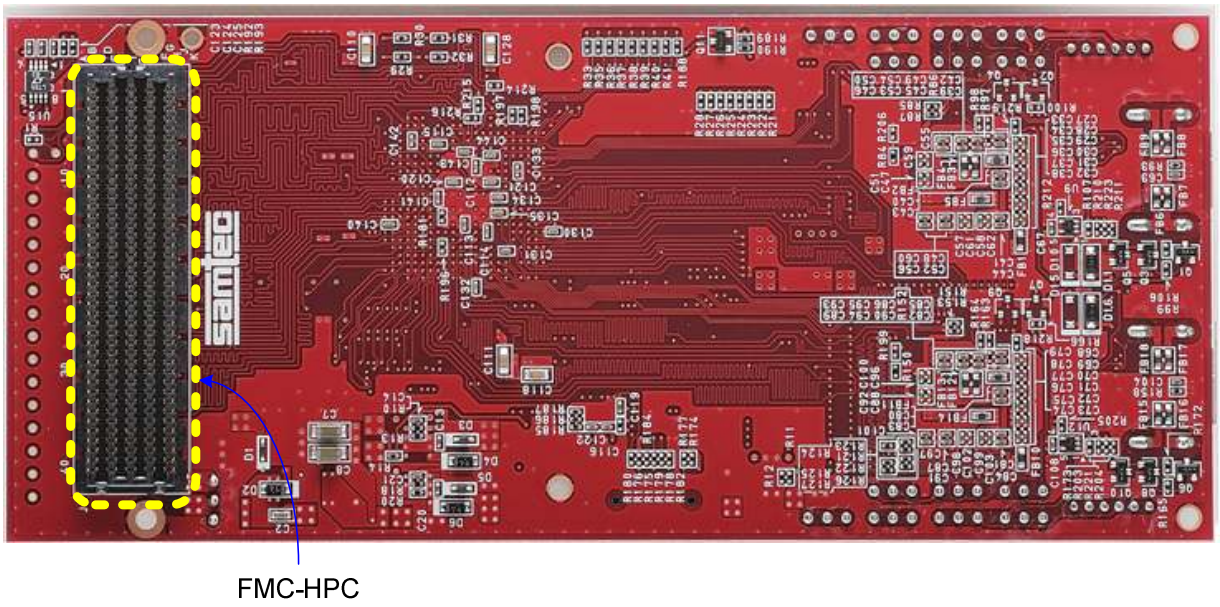

Figure 4-3 External View of TB-FMCH-HDMI2-RX (solder side)

4.3. Board Specification

The following shows TB-FMCH-HDMI2-RX board specifications.

External Dimensions	: W:160mm x H:69mm
Number of Layers	: 8 layers
Board Thickness	: 1.6 mm
Material	: FR-4
FPGA	: Xilinx's XC6SLX45-3FGG484C
FMC Connector	: Samtec's ASP-134488-01
HDMI Connector	: Molex's 5002541927

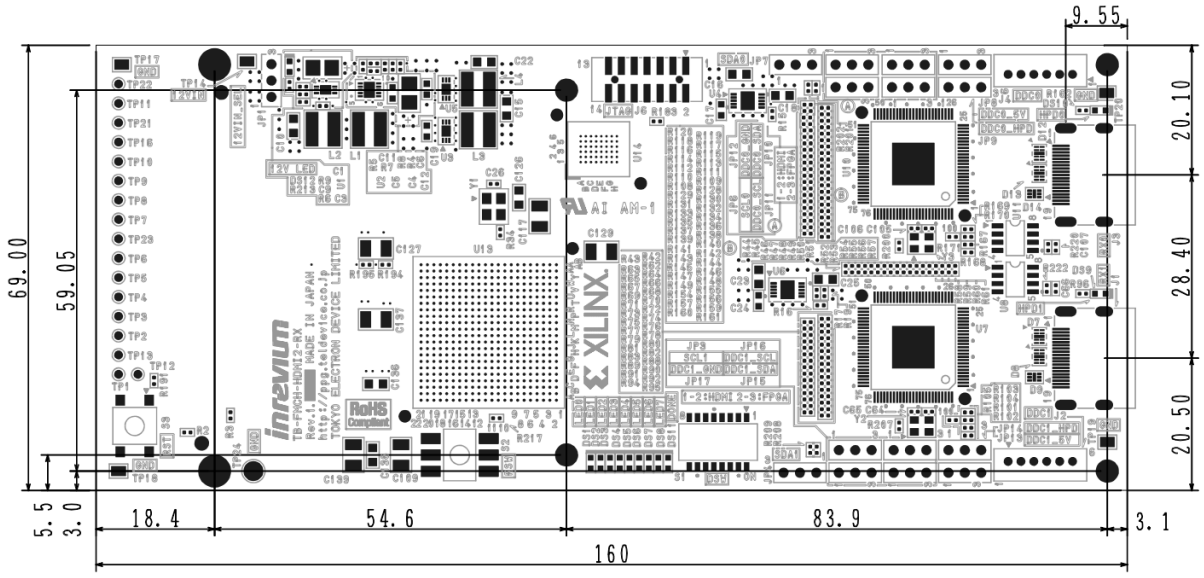

Figure 4-4 TB-FMCH-HDMI2-RX Board Dimensions

4.4. Supplying Power to the Board

Figure 4-5 shows a TB-FMCH-HDMI2-RX power supply structure.

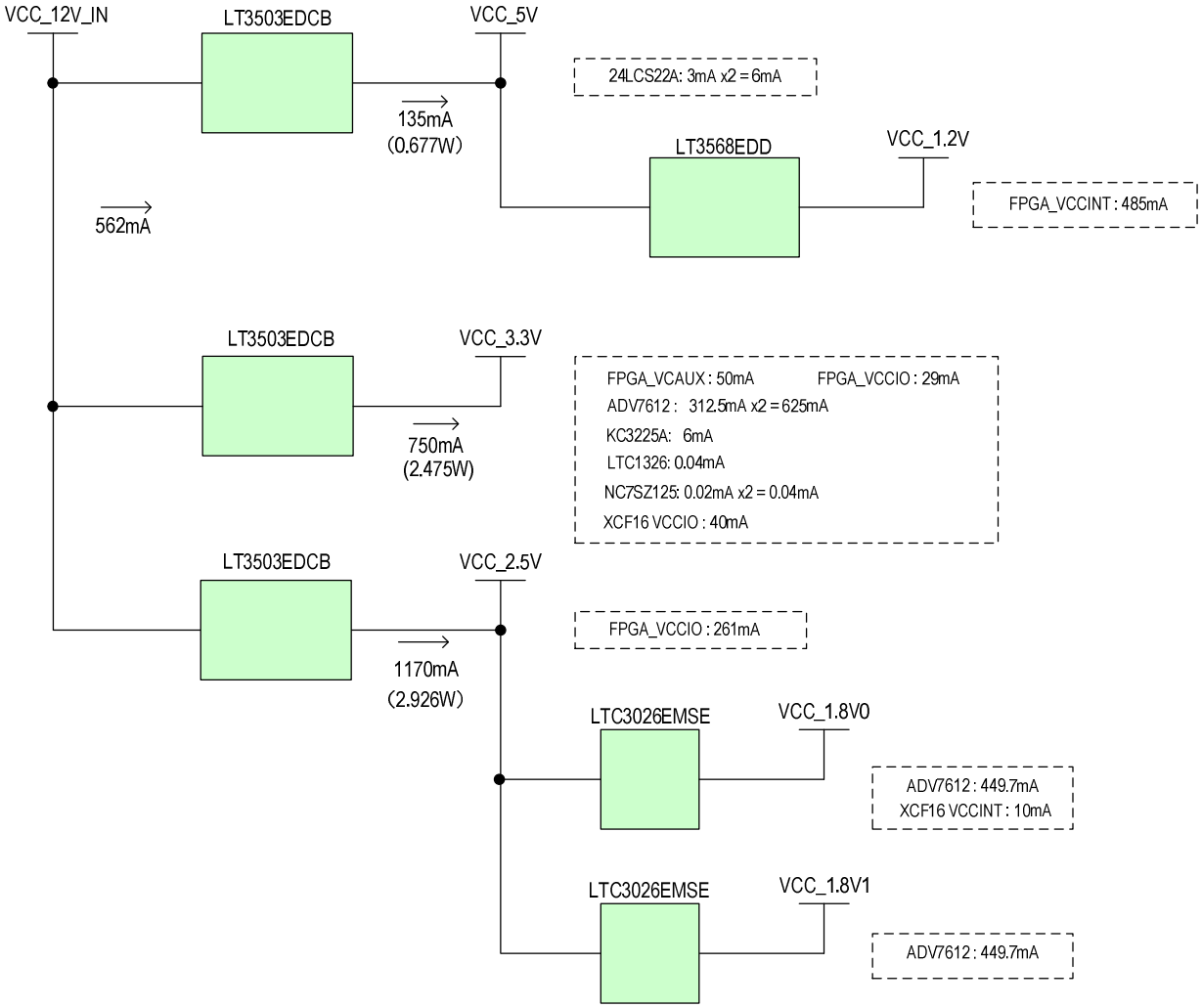

Figure 4-5 TB-FMCH-HDMI2-RX Power Supply Structure

4.5. HDMI Receiver

HDMI Connector uses a 5002541927 (MOLEX).
HDMI Receiver uses an ADV7612BSWZ-P (Analog Devices).
The following device is used as ESD protection.
ESD protection: RCLAMP0524 and RCLAMP0504 (Semtech)
Table 4-1 shows the HDMI connector pin assignments.

Table 4-1 HDMI Connector (receiving side)

Pin #	Name	Description
1	TMDS DATA2+	TMDS receive data 2+
2	TMDS SHLD2	TMDS receive data 2 shield
3	TMDS DATA2-	TMDS receive data 2-
4	TMDS DATA1+	TMDS receive data 1+
5	TMDS SHLD1	TMDS receive data 1 shield
6	TMDS DATA1-	TMDS receive data 1-
7	TMDS DATA0+	TMDS receive data 0+
8	TMDS SHLD0	TMDS receive data 0 shield
9	TMDS DATA0-	TMDS receive data 0-
10	TMDS CLK+	TMDS receive clock+
11	TMDS CLK SHLD	TMDS receive clock shield
12	TMDS CLK-	TMDS receive clock-
13	CEC	CEC signal
14	RESERVED	Reserved
15	DDC_SCL	DDC serial clock
16	DDC_SDA	DDC serial data
17	DDC/CEC GND	DDC/CEC ground
18	DDC_+5V	+5V power supply
19	HOTPLUG_DET	Hot-plug detection

The receiver has an EEPROM (24LCS22A-SN: Micro Chip).
This EEPROM is used to store EDID data. The SCL signal can be switched by JP6/JP3 and the SDA signal using JP7/JP4.

Note: At factory default settings, the EEPROM stores temporary data to enable output of image data from an image output device. The ID used in the data is a dummy ID for evaluation purposes. So, do not use it for actual products.

Table 4-2 SCL/SDA Jumper Setting

No	Purpose	Silk	Setting
1	DDC connection (Normal)	JP6: SCL0, JP7: SDA0 JP3: SCL1,JP4: SDA1	JP6: 1-2 short JP7: 1-2 short JP3: 1-2 short JP4: 1-2 short
2	DDC connection(Through)	JP6: SCL0, JP7: SDA0 JP3: SCL1,JP4: SDA1	JP6: 2-3 short JP7: 2-3 short JP3: 2-3 short JP4: 2-3 short

4.6. FMC Connector

The FMC connector (High-Pin Count) connecting to the main board uses an ASP-134488-01 (SAMTEC).
Power to the TB-FMCH-HDMI2-RX is supplied from a +12V on the main board.
An external power source can also be used.
Table 4-3 shows JP1 jumper setting for power supply.

Table 4-3 JP1 Jumper Setting

No	Purpose	Silk	Setting
1	FMC connector	12VIN_SEL	JP1: 1-2 short
2	External power supply	12VIN_SEL	JP1: 2-3 short

To connect an external power source, use the following test pin:
TP14: 12VIN

Table 4-4 shows the FMC connector pin assignment.

Table 4-4 FMC Connector Pin Assignment

Pin	A-row	B-row	C-row	D-row	E-row
1	GND	RES1	GND	PG_C2M	GND
2	DP1_M2C_P	GND	DP0_C2M_P	GND	HA01_P_CC
3	DP1_M2C_N	GND	DP0_C2M_N	GND	HA01_N_CC
4	GND	DP9_M2C_P	GND	GBTCLK0_M2C_P	GND
5	GND	DP9_M2C_N	GND	GBTCLK0_M2C_N	GND
6	DP2_M2C_P	GND	DP0_M2C_P	GND	HA05_P
7	DP2_M2C_N	GND	DP0_M2C_N	GND	HA05_N
8	GND	DP8_M2C_P	GND	LA01_P_CC	GND
9	GND	DP8_M2C_N	GND	LA01_N_CC	HA09_P
10	DP3_M2C_P	GND	LA06_P	GND	HA09_N
11	DP3_M2C_N	GND	LA06_N	LA05_P	GND
12	GND	DP7_M2C_P	GND	LA05_N	HA13_P
13	GND	DP7_M2C_N	GND	GND	HA13_N
14	DP4_M2C_P	GND	LA10_P	LA09_P	GND
15	DP4_M2C_N	GND	LA10_N	LA09_N	HA16_P
16	GND	DP6_M2C_P	GND	GND	HA16_N
17	GND	DP6_M2C_N	GND	LA13_P	GND
18	DP5_M2C_P	GND	LA14_P	LA13_N	HA20_P
19	DP5_M2C_N	GND	LA14_N	GND	HA20_N
20	GND	GBTCLK1_M2C_P	GND	LA17_P_CC	GND
21	GND	GBTCLK1_M2C_N	GND	LA17_N_CC	HB03_P
22	DP1_C2M_P	GND	LA18_P_CC	GND	HB03_N
23	DP1_C2M_N	GND	LA18_N_CC	LA23_P	GND
24	GND	DP2_C9M_P	GND	LA23_N	HB05_P
25	GND	DP2_C9M_N	GND	GND	HB05_N
26	DP2_C2M_P	GND	LA27_P	LA26_P	GND
27	DP2_C2M_N	GND	LA27_N	LA26_N	HB09_P
28	GND	DP2_C8M_P	GND	GND	HB09_N
29	GND	DP2_C8M_N	GND	TCK	GND
30	DP3_C2M_P	GND	SCL	TDI	HB13_P
31	DP3_C2M_N	GND	SDA	TDO	HB13_N
32	GND	DP2_C7M_P	GND	+3.3VAUX	GND
33	GND	DP2_C7M_N	GND	TMS	HB19_P
34	DP4_C2M_P	GND	GA0	TRST	HB19_N
35	DP4_C2M_N	GND	+12V	GA1	GND
36	GND	DP2_C6M_P	GND	+3.3V	HB21_P
37	GND	DP2_C6M_N	+12V	GND	HB21_N
38	DP5_C2M_P	GND	GND	+3.3V	GND
39	DP5_C2M_N	GND	+3.3V	GND	VADJ
40	GND	RES0	GND	+3.3V	GND

Pin	F-row	G-row	H-row	J-row	K-row
1	PG_M2C	GND	VREF_A_M2C	GND	VREF_B_M2C
2	GND	CLK1_M2C_P	PRSNT_M2C_L	CLK3_M2C_P	GND
3	GND	CLK1_M2C_N	GND	CLK3_M2C_N	GND
4	HA00_P_CC	GND	CLK0_M2C_P	GND	CLK2_M2C_P
5	HA00_N_CC	GND	CLK0_M2C_N	GND	CLK2_M2C_N
6	GND	LA00_P_CC	GND	HA03_P	GND
7	GND	LA00_N_CC	LA02_P	HA03_N	HA02_P
8	HA04_P	GND	LA02_N	GND	HA02_N
9	HA04_N	LA03_P	GND	HA07_P	GND
10	GND	LA03_N	LA04_P	HA07_N	HA06_P
11	HA08_P	GND	LA04_N	GND	HA06_N
12	HA08_N	LA08_P	GND	HA11_P	GND
13	GND	LA08_N	LA07_P	HA11_N	HA10_P
14	HA12_P	GND	LA07_N	GND	HA10_N
15	HA12_N	LA12_P	GND	HA14_P	GND
16	GND	LA12_N	LA11_P	HA14_N	HA17_P_CC
17	HA15_P	GND	LA11_N	GND	HA17_N_CC
18	HA15_N	LA16_P	GND	HA18_P	GND
19	GND	LA16_N	LA15_P	HA18_N	HA21_P
20	HA19_P	GND	LA15_N	GND	HA21_N
21	HA19_N	LA20_P	GND	HA22_P	GND
22	GND	LA20_N	LA19_P	HA22_N	HA23_P
23	HB02_P	GND	LA19_N	GND	HA23_N
24	HB02_N	LA22_P	GND	HB01_P	GND
25	GND	LA22_N	LA21_P	HB01_N	HB00_P_CC
26	HB04_P	GND	LA21_N	GND	HB00_N_CC
27	HB04_N	LA25_P	GND	HB07_P	GND
28	GND	LA25_N	LA24_P	HB07_N	HB06_P_CC
29	HB08_P	GND	LA24_N	GND	HB06_N_CC
30	HB08_N	LA29_P	GND	HB11_P	GND
31	GND	LA29_N	LA28_P	HB11_N	HB10_P
32	HB12_P	GND	LA28_N	GND	HB10_N
33	HB12_N	LA31_P	GND	HB15_P	GND
34	GND	LA31_N	LA30_P	HB15_N	HB14_P
35	HB16_P	GND	LA30_N	GND	HB14_N
36	HB16_N	LA33_P	GND	HB18_P	GND
37	GND	LA33_N	LA32_P	HB18_N	HB17_P_CC
38	HB20_P	GND	LA32_N	GND	HB17_N_CC
39	HB20_N	VADJ	GND	VIO_B_M2C	GND
40	VADJ	GND	VADJ	GND	VIO_B_M2C

4.7. Other Interfaces

The board also has the following interfaces.

4.7.1. EEPROM Interface

I2C interface used to control the EEPROM from the FPGA

EEPROM device: 24LCS22A-SN (Micro Chip)

4.7.2. JTAG Interface

JTAG connector for FPGA configuration

JTAG connector: 87832-1420 (Molex)

Table 4-5 JTAG Connector

Pin	Signal	Pin	Signal
1	GND	2	3.3V
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	NC
13	GND	14	NC

4.7.3. General-Purpose Clock Interface

General-purpose clock for FPGA (27MHz crystal oscillator)

KC5032C027.0000C30E00 (Kyocera)

4.8. LED Status

Table 4-6 shows the onboard LEDs.

Table 4-6 LED Status

No	Circuit #	Silk	Purpose	Description
1	DS1	LED0	General-purpose LED0	[RX0]I2C config state Off: CFG done / On: CFG active
2	DS2	LED1	General-purposeLED1	[RX0]I2C read back Off: Error / On: No error
3	DS3	LED2	General-purposeLED2	[RX0]Video status LED2: OFF, LED3: OFF : 2D Video LED2: ON, LED3: OFF : 3D SideBySide LED2: OFF, LED3: ON : 3D TopAndBottom LED2: ON, LED3: ON : 3D FramePacking
4	DS4	LED3	General-purposeLED3	
5	DS5	LED4	General-purposeLED4	Unused (On)
6	DS6	LED5	General-purposeLED5	[RX0] Input video image clock monitor Flashing: Clock / Off: No clock
7	DS7	LED6	General-purposeLED6	Unused (On)
8	DS8	LED7	General-purposeLED7	System reset monitor On: Reset active / Off: Reset released
9	DS10	HPD0	RX0 hot-plug display	On: Connected state
10	DS9	HPD1	RX1 hot-plug display	On: Connected state
11	DS11	DONE	Config display	On: Config done
12	DS12	12VLED	12V display	On: 12V active

4.9. Control Function

Table 4-7 shows the onboard switch function.

Table 4-7 Switches

No	Circuit #	Silk	Function
1	S1-1	DSW	ADV7612 config ROM selection *Please refer to Table 4-8.
2	S1-2	DSW	
3	S1-3	DSW	
4	S1-4	DSW	
5	S1-5	DSW	Unused *set to ON
6	S1-6	DSW	Unused *set to ON
7	S1-7	DSW	Unused *set to ON
8	S1-8	DSW	Unused *set to ON
9	S2	RSW	Unused *set to '0'.
10	S3	RST	FPGA reconfig (long push: 3 seconds) FPGA reset (short push)

4.9.1. ADV7612 Configuration ROM selection

Table 4-8 shows the configuration ROM function and settings for ADV7612.

Table 4-8 ADV7612 configuration ROM

No	DSW (S1-4)	DSW (S1-3)	DSW (S1-2)	DSW (S1-1)	Color format
1	ON	ON	ON	ON	Color Space:YCbCr 444/422, Color Depth:8bit
2	ON	ON	ON	OFF	Color Space:YCbCr 444/422, Color Depth:10bit
3	ON	ON	OFF	ON	Color Space:YCbCr 444/422, Color Depth:12bit
4	ON	ON	OFF	OFF	-
5	ON	OFF	ON	ON	Color Space:RGB, Color Depth:8bit
6	ON	OFF	ON	OFF	Color Space:RGB, Color Depth:10bit
7	ON	OFF	OFF	ON	Color Space:RGB, Color Depth:12bit
8	ON	OFF	OFF	OFF	-
9	OFF	ON	ON	ON	-
10	OFF	ON	ON	OFF	-
11	OFF	ON	OFF	ON	-
12	OFF	ON	OFF	OFF	-
13	OFF	OFF	ON	ON	-
14	OFF	OFF	ON	OFF	-
15	OFF	OFF	OFF	ON	-
16	OFF	OFF	OFF	OFF	-

4.10. FPGA Pin Assignment

Table 4-9 shows the FPGA pin assignment.

In case of 8-bit signal format, active bits are assigned to MSB 8-bit of each RGB pin of FMC. LSB 2-bit are always 2'b00 in 8-bit signal format.

Table 4-9 FPGA Pin Assignment

Pin Name	No.	IO	Spec	Description
CLK0_M2C_P	B10	O	LVCMOS25	RX#0_LLC signal (FPGA to FMC)
CLK1_M2C_P	C11	O	LVCMOS25	Unused
LA00_P_CC	D6	O	LVCMOS25	RX#0_VSYNC signal (FPGA to FMC)
LA01_P_CC	C7	O	LVCMOS25	RX#0_HSYNC signal (FPGA to FMC)
LA02_P	D9	O	LVCMOS25	RX#0_DE signal (FPGA to FMC)
LA03_P	D7	O	LVCMOS25	RX#0_P0 signal (FPGA to FMC) [Cb0/B0]
LA04_P	C13	O	LVCMOS25	RX#0_P1 signal (FPGA to FMC) [Cb1/B1]
LA05_P	B14	O	LVCMOS25	RX#0_P2 signal (FPGA to FMC) [Cb2/B2]
LA06_P	D15	O	LVCMOS25	RX#0_P3 signal (FPGA to FMC) [Cb3/B3]
LA07_P	C17	O	LVCMOS25	RX#0_P4 signal (FPGA to FMC) [Cb4/B4]
LA08_P	E16	O	LVCMOS25	RX#0_P5 signal (FPGA to FMC) [Cb5/B5]
LA09_P	G16	O	LVCMOS25	RX#0_P6 signal (FPGA to FMC) [Cb6/B6]
LA10_P	B21	O	LVCMOS25	RX#0_P7 signal (FPGA to FMC) [Cb7/B7]
LA11_P	K16	O	LVCMOS25	RX#0_P8 signal (FPGA to FMC) [Cb8/B8]
LA12_P	D19	O	LVCMOS25	RX#0_P9 signal (FPGA to FMC) [Cb9/B9]
LA13_P	D21	O	LVCMOS25	RX#0_P10 signal (FPGA to FMC) [Y10/G10]
LA14_P	G19	O	LVCMOS25	RX#0_P11 signal (FPGA to FMC) [Y11/G11]
LA15_P	E20	O	LVCMOS25	RX#0_P12 signal (FPGA to FMC) [Y0/G0]
LA16_P	F21	O	LVCMOS25	RX#0_P13 signal (FPGA to FMC) [Y1/G1]
LA17_P_CC	G20	O	LVCMOS25	RX#0_P14 signal (FPGA to FMC) [Y2/G2]
LA18_P_CC	H21	O	LVCMOS25	RX#0_P15 signal (FPGA to FMC) [Y3/G3]
LA19_P	J20	O	LVCMOS25	RX#0_P16 signal (FPGA to FMC) [Y4/G4]
LA20_P	L20	O	LVCMOS25	RX#0_P17 signal (FPGA to FMC) [Y5/G5]
LA21_P	N20	O	LVCMOS25	RX#0_P18 signal (FPGA to FMC) [Y6/G6]
LA22_P	R20	O	LVCMOS25	RX#0_P19 signal (FPGA to FMC) [Y7/G7]
LA23_P	U20	O	LVCMOS25	RX#0_P20 signal (FPGA to FMC) [Y8/G8]
LA24_P	M19	O	LVCMOS25	RX#0_P21 signal (FPGA to FMC) [Y9/G9]
LA25_P	M16	O	LVCMOS25	RX#0_P22 signal (FPGA to FMC) [Cr0/R0]
LA26_P	P19	O	LVCMOS25	RX#0_P23 signal (FPGA to FMC) [Cr1/R1]
LA27_P	W20	O	LVCMOS25	RX#0_P24 signal (FPGA to FMC) [Cr2/R2]
LA28_P	L17	O	LVCMOS25	RX#0_P25 signal (FPGA to FMC) [Cr3/R3]
LA29_P	U19	O	LVCMOS25	RX#0_P26 signal (FPGA to FMC) [Cr4/R4]
LA30_P	M17	O	LVCMOS25	RX#0_P27 signal (FPGA to FMC) [Cr5/R5]
LA31_P	P17	O	LVCMOS25	RX#0_P28 signal (FPGA to FMC) [Cr6/R6]
LA32_P	P18	O	LVCMOS25	RX#0_P29 signal (FPGA to FMC) [Cr7/R7]
LA33_P	T19	IO	LVCMOS25	Unused
CLK0_M2C_N	A10	IO	LVCMOS25	Unused
CLK1_M2C_N	A11	IO	LVCMOS25	unused

Pin Name	No.	IO	Spec	Description
LA00_N_CC	C6	O	LVCMOS25	RX#0_input video status[0] (FPGA to FMC)
LA01_N_CC	A7	O	LVCMOS25	RX#0_input video status[1] (FPGA to FMC) *Please see Note
LA02_N	C8	O	LVCMOS25	Unused
LA03_N	D8	O	LVCMOS25	Unused
LA04_N	A13	O	LVCMOS25	Unused
LA05_N	A14	O	LVCMOS25	Unused
LA06_N	C16	O	LVCMOS25	Unused
LA07_N	A17	O	LVCMOS25	Unused
LA08_N	D17	O	LVCMOS25	Unused
LA09_N	G17	O	LVCMOS25	Unused
LA10_N	B22	O	LVCMOS25	Unused
LA11_N	J16	O	LVCMOS25	Unused
LA12_N	D20	O	LVCMOS25	Unused
LA13_N	D22	O	LVCMOS25	Unused
LA14_N	F20	O	LVCMOS25	Unused
LA15_N	E22	O	LVCMOS25	Unused
LA16_N	F22	O	LVCMOS25	Unused
LA17_N_CC	G22	O	LVCMOS25	Unused
LA18_N_CC	H22	O	LVCMOS25	Unused
LA19_N	J22	O	LVCMOS25	RX#0_MCLK signal (FPGA to FMC)
LA20_N	L22	O	LVCMOS25	RX#0_SCLK signal (FPGA to FMC)
LA21_N	N22	O	LVCMOS25	RX#0_AP0 signal (FPGA to FMC)
LA22_N	R22	O	LVCMOS25	RX#0_AP1 signal (FPGA to FMC)
LA23_N	U22	O	LVCMOS25	RX#0_AP2 signal (FPGA to FMC)
LA24_N	N19	O	LVCMOS25	RX#0_AP3 signal (FPGA to FMC)
LA25_N	L15	O	LVCMOS25	RX#0_AP4 signal (FPGA to FMC)
LA26_N	P20	O	LVCMOS25	RX#0_AP5 signal (FPGA to FMC)
LA27_N	W22	O	LVCMOS25	RX#0_P30 signal (FPGA to FMC) [Cr6/R6]
LA28_N	K18	O	LVCMOS25	RX#0_P31 signal (FPGA to FMC) [Cr7/R7]
LA29_N	V20	O	LVCMOS25	RX#0_P32 signal (FPGA to FMC) [Cr8/R8]
LA30_N	M18	O	LVCMOS25	RX#0_P33 signal (FPGA to FMC) [Cr9/R9]
LA31_N	N16	O	LVCMOS25	RX#0_P34 signal (FPGA to FMC) [Cr10/R10]
LA32_N	R19	O	LVCMOS25	RX#0_P35 signal (FPGA to FMC) [Cr11/R11]
LA33_N	T20	IO	LVCMOS25	Unused
CLK2_M2C_P	D11	IO	LVCMOS25	Unused
CLK3_M2C_P	B12	IO	LVCMOS25	Unused
HA00_P_CC	B6	IO	LVCMOS25	Unused
HA01_P_CC	B8	IO	LVCMOS25	Unused
HA02_P	C9	IO	LVCMOS25	Unused
HA03_P	D10	IO	LVCMOS25	Unused
HA04_P	D14	IO	LVCMOS25	Unused
HA05_P	C15	IO	LVCMOS25	Unused

Pin Name	No.	IO	Spec	Description
HA06_P	B16	IO	LVCMOS25	unused
HA07_P	B18	IO	LVCMOS25	unused
HA08_P	C19	IO	LVCMOS25	unused
HA09_P	F16	IO	LVCMOS25	unused
HA10_P	A20	IO	LVCMOS25	unused
HA11_P	H16	IO	LVCMOS25	unused
HA12_P	F18	IO	LVCMOS25	unused
HA13_P	C20	IO	LVCMOS25	unused
HA14_P	H19	IO	LVCMOS25	unused
HA15_P	J17	IO	LVCMOS25	unused
HA16_P	H20	IO	LVCMOS25	unused
HA17_P_CC	K20	IO	LVCMOS25	unused
HA18_P	M20	IO	LVCMOS25	unused
HA19_P	K21	IO	LVCMOS25	unused
HA20_P	M21	IO	LVCMOS25	unused
HA21_P	P21	IO	LVCMOS25	unused
HA22_P	T21	IO	LVCMOS25	unused
HA23_P	V21	IO	LVCMOS25	unused
CLK2_M2C_N	C12	IO	LVCMOS25	unused
CLK3_M2C_N	A12	IO	LVCMOS25	unused
HA00_N_CC	A6	IO	LVCMOS25	unused
HA01_N_CC	A8	IO	LVCMOS25	unused
HA02_N	A9	IO	LVCMOS25	unused
HA03_N	C10	IO	LVCMOS25	unused
HA04_N	C14	IO	LVCMOS25	unused
HA05_N	A15	IO	LVCMOS25	unused
HA06_N	A16	IO	LVCMOS25	unused
HA07_N	A18	IO	LVCMOS25	unused
HA08_N	B20	IO	LVCMOS25	unused
HA09_N	F17	IO	LVCMOS25	unused
HA10_N	A21	IO	LVCMOS25	unused
HA11_N	H17	IO	LVCMOS25	unused
HA12_N	F19	IO	LVCMOS25	unused
HA13_N	C22	IO	LVCMOS25	unused
HA14_N	H18	IO	LVCMOS25	unused
HA15_N	K17	IO	LVCMOS25	unused
HA16_N	J19	IO	LVCMOS25	unused
HA17_N_CC	K19	IO	LVCMOS25	unused
HA18_N	L19	IO	LVCMOS25	unused
HA19_N	K22	IO	LVCMOS25	unused
HA20_N	M22	IO	LVCMOS25	unused
HA21_N	P22	IO	LVCMOS25	unused

Pin Name	No.	IO	Spec	Description
HA22_N	T22	IO	LVCMOS25	unused
HA23_N	V22	IO	LVCMOS25	unused
RX#0_P35	T18	I	LVCMOS33	RX#0 Video data 35 (RX to FPGA)
RX#0_P34	T17	I	LVCMOS33	RX#0 Video data 34 (RX to FPGA)
RX#0_P33	Y19	I	LVCMOS33	RX#0 Video data 33 (RX to FPGA)
RX#0_P32	AB19	I	LVCMOS33	RX#0 Video data 32 (RX to FPGA)
RX#0_P31	W18	I	LVCMOS33	RX#0 Video data 31 (RX to FPGA)
RX#0_P30	Y18	I	LVCMOS33	RX#0 Video data 30 (RX to FPGA)
RX#0_P29	T16	I	LVCMOS33	RX#0 Video data 29 (RX to FPGA)
RX#0_P28	T15	I	LVCMOS33	RX#0 Video data 28 (RX to FPGA)
RX#0_P27	U17	I	LVCMOS33	RX#0 Video data 27 (RX to FPGA)
RX#0_P26	U16	I	LVCMOS33	RX#0 Video data 26 (RX to FPGA)
RX#0_P25	V19	I	LVCMOS33	RX#0 Video data 25 (RX to FPGA)
RX#0_P24	V18	I	LVCMOS33	RX#0 Video data 24 (RX to FPGA)
RX#0_P23	R16	I	LVCMOS33	RX#0 Video data 23 (RX to FPGA)
RX#0_P22	R15	I	LVCMOS33	RX#0 Video data 22 (RX to FPGA)
RX#0_P21	V17	I	LVCMOS33	RX#0 Video data 21 (RX to FPGA)
RX#0_P20	W17	I	LVCMOS33	RX#0 Video data 20 (RX to FPGA)
RX#0_P19	V15	I	LVCMOS33	RX#0 Video data 19 (RX to FPGA)
RX#0_P18	AA18	I	LVCMOS33	RX#0 Video data 18 (RX to FPGA)
RX#0_P17	AB18	I	LVCMOS33	RX#0 Video data 17 (RX to FPGA)
RX#0_P16	Y17	I	LVCMOS33	RX#0 Video data 16 (RX to FPGA)
RX#0_P15	AB17	I	LVCMOS33	RX#0 Video data 15 (RX to FPGA)
RX#0_P14	AA14	I	LVCMOS33	RX#0 Video data 14 (RX to FPGA)
RX#0_P13	AB14	I	LVCMOS33	RX#0 Video data 13 (RX to FPGA)
RX#0_P12	Y16	I	LVCMOS33	RX#0 Video data 12 (RX to FPGA)
RX#0_P11	W15	I	LVCMOS33	RX#0 Video data 11 (RX to FPGA)
RX#0_P10	V13	I	LVCMOS33	RX#0 Video data 10 (RX to FPGA)
RX#0_P9	W13	I	LVCMOS33	RX#0 Video data 9 (RX to FPGA)
RX#0_P8	AA16	I	LVCMOS33	RX#0 Video data 8 (RX to FPGA)
RX#0_P7	AB16	I	LVCMOS33	RX#0 Video data 7 (RX to FPGA)
RX#0_P6	W14	I	LVCMOS33	RX#0 Video data 6 (RX to FPGA)
RX#0_P5	Y14	I	LVCMOS33	RX#0 Video data 5 (RX to FPGA)
RX#0_P4	Y15	I	LVCMOS33	RX#0 Video data 4 (RX to FPGA)
RX#0_P3	AB15	I	LVCMOS33	RX#0 Video data 3 (RX to FPGA)
RX#0_P2	T12	I	LVCMOS33	RX#0 Video data 2 (RX to FPGA)
RX#0_P1	U12	I	LVCMOS33	RX#0 Video data 1 (RX to FPGA)
RX#0_P0	T14	I	LVCMOS33	RX#0 Video data 0 (RX to FPGA)
RX#0_DE	R13	I	LVCMOS33	RX#0 data enable (RX to FPGA)
RX#0_LLC	W12	I	LVCMOS33	RX#0 LLC signal (RX to FPGA)
RX#0_SCLK	Y13	I	LVCMOS33	RX#0 Audio serial clock (RX to FPGA)
RX#0_MCLKOUT	AA12	I	LVCMOS33	RX#0 Audio master clock (RX to FPGA)

Pin Name	No.	IO	Spec	Description
SYSCLK_P	Y11	I	LVCMOS33	System Clock (27MHz)
RX#0_HSYNC	R11	I	LVCMOS33	RX#0 HSYNC (RX to FPGA)
RX#0_VSYNC	T11	I	LVCMOS33	RX#0 VSYNC (RX to FPGA)
RX#0_SPDIF	AA10	I	LVCMOS33	RX#0 SPDIF Digital Audio (RX to FPGA)
RX#0_I2S0	AB10	I	LVCMOS33	RX#0 I2S Audio Signal 0 (RX to FPGA)
RX#0_I2S1	V11	I	LVCMOS33	RX#0 I2S Audio Signal 1 (RX to FPGA)
RX#0_I2S2	W11	I	LVCMOS33	RX#0 I2S Audio Signal 2 (RX to FPGA)
RX#0_I2S3	Y9	I	LVCMOS33	RX#0 I2S Audio Signal 3 (RX to FPGA)
RX#0_LRCLK	AB9	I	LVCMOS33	RX#0 LRCLK Signal (RX to FPGA)
RX#0_SCL	W10	O	LVCMOS33	RX#0 I2C Serial Clock (FPGA to RX)
RX#0_SDA	Y10	IO	LVCMOS33	RX#0 I2C Serial Data (RX to/from FPGA)
RX#0_INT1	AA8	I	LVCMOS33	RX#0 Interrupt Input 1 (RX to FPGA)
RX#0_RESETN	AB8	O	LVCMOS33	RX#0 Reset (FPGA to RX)
RX#0_CSN	W8	O	LVCMOS33	RX#0 CS Output (FPGA to RX)
RX#0_CEC	V7	IO	LVCMOS33	RX#0 CEC Signal (RX to/from FPGA)
RX#0_DDCA_SCL_F	W9	I	LVCMOS33	RX#0 DDC Serial Clock (RX to FPGA)
RX#0_DDCA_SDA_F	Y8	IO	LVCMOS33	RX#0 DDC Serial Data (RX to/from FPGA)
RX#0_HPD_IO	U9	O	LVCMOS33	RX#0 Hot Plug Control (FPGA to RX)
RX#0_DET1	V9	I	LVCMOS33	RX#0 Detect Signal (RX to FPGA)
FPGA_SRSTN	AA2	I	LVCMOS33	FPGA Reset
RX#1_P35	Y2	I	LVCMOS33	RX#1 Video Data 35 (RX to FPGA)
RX#1_P34	Y1	I	LVCMOS33	RX#1 Video Data 34 (RX to FPGA)
RX#1_P33	W3	I	LVCMOS33	RX#1 Video Data 33 (RX to FPGA)
RX#1_P32	W1	I	LVCMOS33	RX#1 Video Data 32 (RX to FPGA)
RX#1_P31	P8	I	LVCMOS33	RX#1 Video Data 31 (RX to FPGA)
RX#1_P30	P7	I	LVCMOS33	RX#1 Video Data 30 (RX to FPGA)
RX#1_P29	P6	I	LVCMOS33	RX#1 Video Data 29 (RX to FPGA)
RX#1_P28	P5	I	LVCMOS33	RX#1 Video Data 28 (RX to FPGA)
RX#1_P27	T4	I	LVCMOS33	RX#1 Video Data 27 (RX to FPGA)
RX#1_P26	T3	I	LVCMOS33	RX#1 Video Data 26 (RX to FPGA)
RX#1_P25	U4	I	LVCMOS33	RX#1 Video Data 25 (RX to FPGA)
RX#1_P24	V3	I	LVCMOS33	RX#1 Video Data 24 (RX to FPGA)
RX#1_P23	N6	I	LVCMOS33	RX#1 Video Data 23 (RX to FPGA)
RX#1_P22	N7	I	LVCMOS33	RX#1 Video Data 22 (RX to FPGA)
RX#1_P21	M7	I	LVCMOS33	RX#1 Video Data 21 (RX to FPGA)
RX#1_P20	M8	I	LVCMOS33	RX#1 Video Data 20 (RX to FPGA)
RX#1_P19	R4	I	LVCMOS33	RX#1 Video Data 19 (RX to FPGA)
RX#1_P18	P4	I	LVCMOS33	RX#1 Video Data 18 (RX to FPGA)
RX#1_P17	M6	I	LVCMOS33	RX#1 Video Data 17 (RX to FPGA)
RX#1_P16	L6	I	LVCMOS33	RX#1 Video Data 16 (RX to FPGA)
RX#1_P15	P3	I	LVCMOS33	RX#1 Video Data 15 (RX to FPGA)
RX#1_P14	N4	I	LVCMOS33	RX#1 Video Data 14 (RX to FPGA)

Pin Name	No.	IO	Spec	Description
RX#1_P13	M5	I	LVCMOS33	RX#1 Video Data 13 (RX to FPGA)
RX#1_P12	M4	I	LVCMOS33	RX#1 Video Data 12 (RX to FPGA)
RX#1_P11	V2	I	LVCMOS33	RX#1 Video Data 11 (RX to FPGA)
RX#1_P10	V1	I	LVCMOS33	RX#1 Video Data 10 (RX to FPGA)
RX#1_P9	U3	I	LVCMOS33	RX#1 Video Data 9 (RX to FPGA)
RX#1_P8	U1	I	LVCMOS33	RX#1 Video Data 8 (RX to FPGA)
RX#1_P7	T2	I	LVCMOS33	RX#1 Video Data 7 (RX to FPGA)
RX#1_P6	T1	I	LVCMOS33	RX#1 Video Data 6 (RX to FPGA)
RX#1_P5	R3	I	LVCMOS33	RX#1 Video Data 5 (RX to FPGA)
RX#1_P4	R1	I	LVCMOS33	RX#1 Video Data 4 (RX to FPGA)
RX#1_P3	P2	I	LVCMOS33	RX#1 Video Data 3 (RX to FPGA)
RX#1_P2	P1	I	LVCMOS33	RX#1 Video Data 2 (RX to FPGA)
RX#1_P1	N3	I	LVCMOS33	RX#1 Video Data 1 (RX to FPGA)
RX#1_P0	N1	I	LVCMOS33	RX#1 Video Data 0 (RX to FPGA)
RX#1_DE	M2	I	LVCMOS33	RX#1 Data Enable (RX to FPGA)
RX#1_LLC	J3	I	LVCMOS33	RX#1 LLC Signal (RX to FPGA)
RX#1_SCLK	M3	I	LVCMOS33	RX#1 Audio Serial Clock (RX to FPGA)
RX#1_MCLKOUT	K5	I	LVCMOS33	RX#1 Audio Master Clock (RX to FPGA)
RX#1_HSYNC	M1	I	LVCMOS33	RX#1 HSYNC (RX to FPGA)
RX#1_VSYNC	L3	I	LVCMOS33	RX#1 VSYNC (RX to FPGA)
RX#1_SPDIF	L1	I	LVCMOS33	RX#1 SPDIF Digital Audio (RX to FPGA)
RX#1_I2S0	K2	I	LVCMOS33	RX#1 I2S Audio Signal 0 (RX to FPGA)
RX#1_I2S1	K1	I	LVCMOS33	RX#1 I2S Audio Signal 1 (RX to FPGA)
RX#1_I2S2	K6	I	LVCMOS33	RX#1 I2S Audio Signal 2 (RX to FPGA)
RX#1_I2S3	J6	I	LVCMOS33	RX#1 I2S Audio Signal 3 (RX to FPGA)
RX#1_LRCLK	H4	I	LVCMOS33	RX#1 LRCLK Signal (RX to FPGA)
RX#1_SCL	H3	O	LVCMOS33	RX#1 I2C Serial Clock (FPGA to RX)
RX#1_SDA	H2	IO	LVCMOS33	RX#1 I2C Serial Data (RX to/from FPGA)
RX#1_INT1	H1	I	LVCMOS33	RX#1 Interrupt Input 1 (RX to FPGA)
RX#1_RESETN	G3	O	LVCMOS33	RX#1 Reset (FPGA to RX)
RX#1_CSN	G1	O	LVCMOS33	RX#1 CS Output (FPGA to RX)
RX#1_CEC	H6	IO	LVCMOS33	RX#1 CEC Signal (RX to/from FPGA)
RX#1_DDCA_SCL_F	H5	I	LVCMOS33	RX#1 DDC Serial Clock (RX to FPGA)
RX#1_DDCA_SDA_F	F2	IO	LVCMOS33	RX#1 DDC Serial Data (RX<=>FPGA)
RX#1_HPD_IO	F1	O	LVCMOS33	RX#1 Hot Plug Control (FPGA to RX)
RX#1_DET1	G4	I	LVCMOS33	RX#1 Detect Signal (RX to FPGA)
RSW0	D2	I	LVCMOS33	Rotary Switch 0
RSW1	D1	I	LVCMOS33	Rotary Switch 1
RSW2	C3	I	LVCMOS33	Rotary Switch 2
RSW3	C1	I	LVCMOS33	Rotary Switch 3
DSW0	F5	I	LVCMOS33	DIP Switch 0
DSW1	K7	I	LVCMOS33	DIP Switch 1

Pin Name	No.	IO	Spec	Description
DSW2	K8	I	LVCMOS33	DIP Switch 2
DSW3	D5	I	LVCMOS33	DIP Switch 3
DSW4	E4	I	LVCMOS33	DIP Switch 4
DSW5	J7	I	LVCMOS33	DIP Switch 5
DSW6	H8	I	LVCMOS33	DIP Switch 6
DSW7	B2	I	LVCMOS33	DIP Switch 7
LED0	G7	O	LVCMOS33	LED0
LED1	F7	O	LVCMOS33	LED1
LED2	D3	O	LVCMOS33	LED2
LED3	C4	O	LVCMOS33	LED3
LED4	E5	O	LVCMOS33	LED4
LED5	E6	O	LVCMOS33	LED5
LED6	A2	O	LVCMOS33	LED6
LED7	B3	O	LVCMOS33	LED7

Note: Input Video Status[1:0]

This status shows 2D / 3D video format.

[1:0] = “00” : 2D video.

[1:0] = “01” : 3D video. SideBySide format.

[1:0] = “10” : 3D video. TopAndBottom format.

[1:0] = “11” : 3D video. FramePacking format.

4.11. FPGA Output Data Phase

Figure 4-6 shows the output data phase of FPGA on TB-FMCH-HDMI2-RX.
FPGA to FMC data is output at the falling edge of the video clock.
The data should be latched at the rising edge on the main board side.

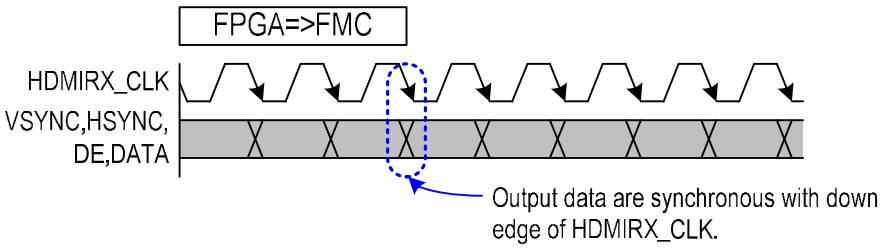

Figure 4-6 FPGA Output Data Timing

4.12. Audio(I2S format)

This design supports I2S format audio. Figure 4-7 shows audio output timing chart.
FPGA does not synchronaise audio signals from ADV7612.

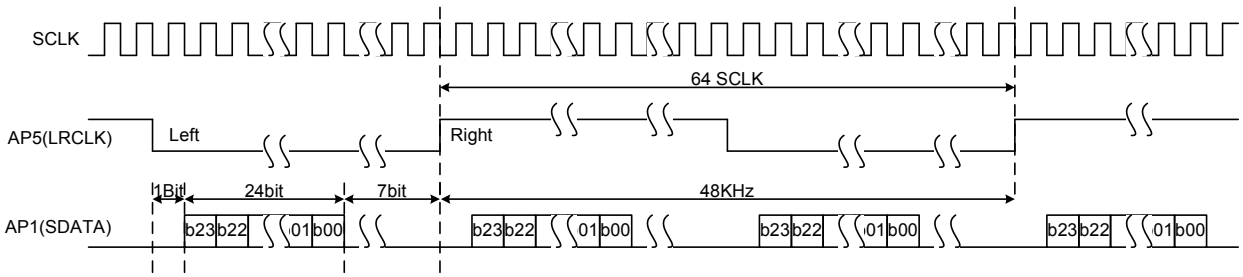

Figure 4-7 I2S Format Audio Timing Chart

4.13. Image Size

4.13.1. 2D Image Size

TB-FMCH-HDMI2-RX supports HDMI1.4-compliant primary format and part of secondary format (1080p@60Hz).

Supported image size:

- 640x480p@59.94/60Hz
- 1280x720p@59.94/60Hz
- 1920x1080i@59.94/60Hz
- 720x480p @ 59.94/60Hz
- 720(1440)x480i@59.94/60Hz
- 1280x720@50Hz
- 1920x1080i@50Hz
- 720x576p@50Hz
- 720(1440)x576i@50Hz
- 1920x1080p@59.94/60Hz
- 1920x1080p@50Hz

4.13.2. 3D Image Size

TB-FMCH-HDMI2-RX supports HDMI1.4-compliant primary format.

Supported image size:

- 1280x720p@59.94/60Hz (Frame Packing, Side-by-Side(Half), Top-and-Bottom)
- 1280x720p@50Hz (Frame Packing, Side-by-Side(Half), Top-and-Bottom)
- 1280x720p@23.98/24Hz (Frame Packing)
- 1280x720p@23.97/30Hz (Frame Packing)
- 1920x1080i@59.94/60Hz (Frame Packing, Side-by-Side(Half))
- 1920x1080i@50Hz (Frame Packing, Side-by-Side(Half))
- 1920x1080p@23.98/24Hz (Frame Packing, Side-by-Side(Half), Top-and-Bottom)
- 1920x1080p@29.97/30Hz (Frame Packing, Top-and-Bottom)
- 1920x1080p@59.94/60Hz (Top-and-Bottom)
- 1920x1080p@50Hz (Top-and-Bottom)

5. TB-FMCH-HDMI2-TX

5.1. Block Diagram

Figure 5-1 shows a TB-FMCH-HDMI2-TX block diagram.

The FMC-HPC connector is mounted on the solder side of the board.

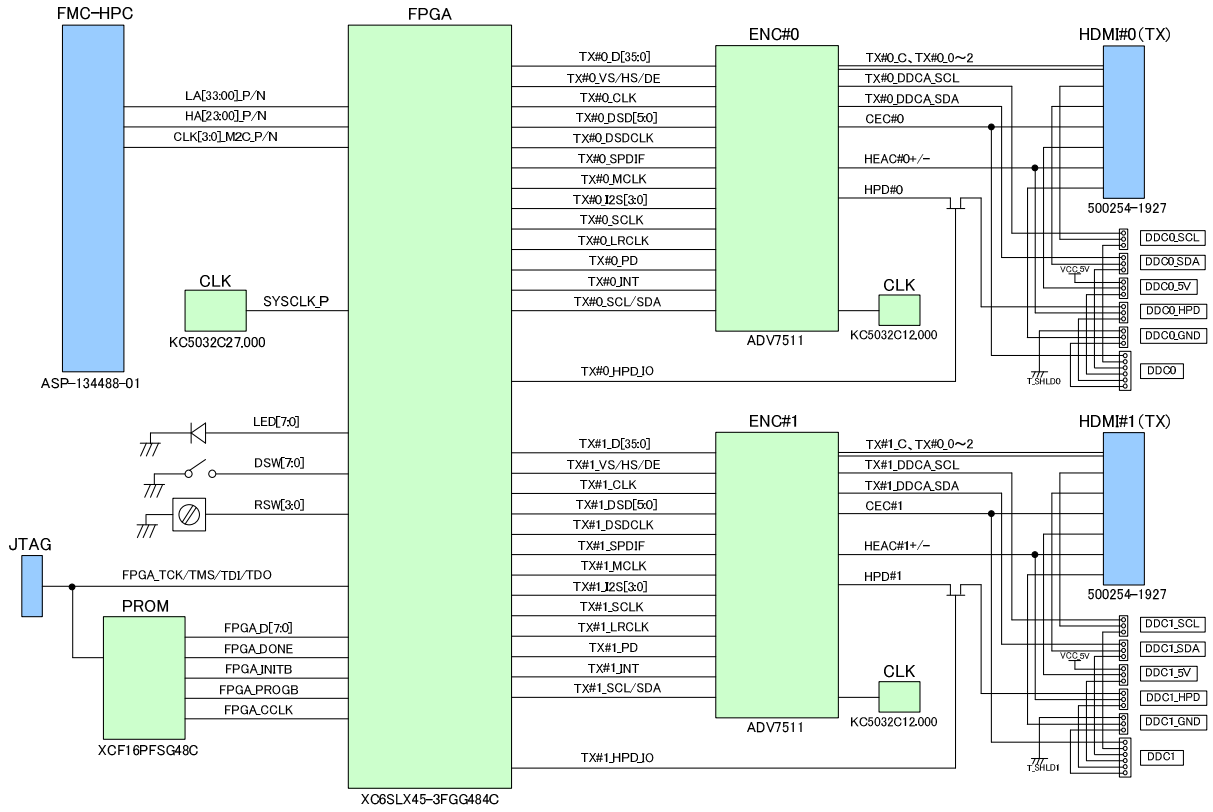

Figure 5-1 TB-FMCH-HDMI2-TX Block Diagram

Main Function:

1. HDMI Transmit (FPGA to ADV7511)
2. FMC Connector Interface (FMC-HPC to FPGA)
3. JTAG Interface
4. General-purpose Clock Interface (27MHz)
5. General-purpose Switch
6. General-purpose LED
7. DDC Connection (Normal/ Through)

Note: This design uses HDMI#0(TX) only. Because of limited pin number of FMC-LPC.

5.2. External View of the Board

Figures 5-2 and 5-3 show the external view of the TB-FMCH-HDMI2-TX board.

Caution : This board has a plastic cover for protecting HDMI devices. Do not remove a plastic cover.

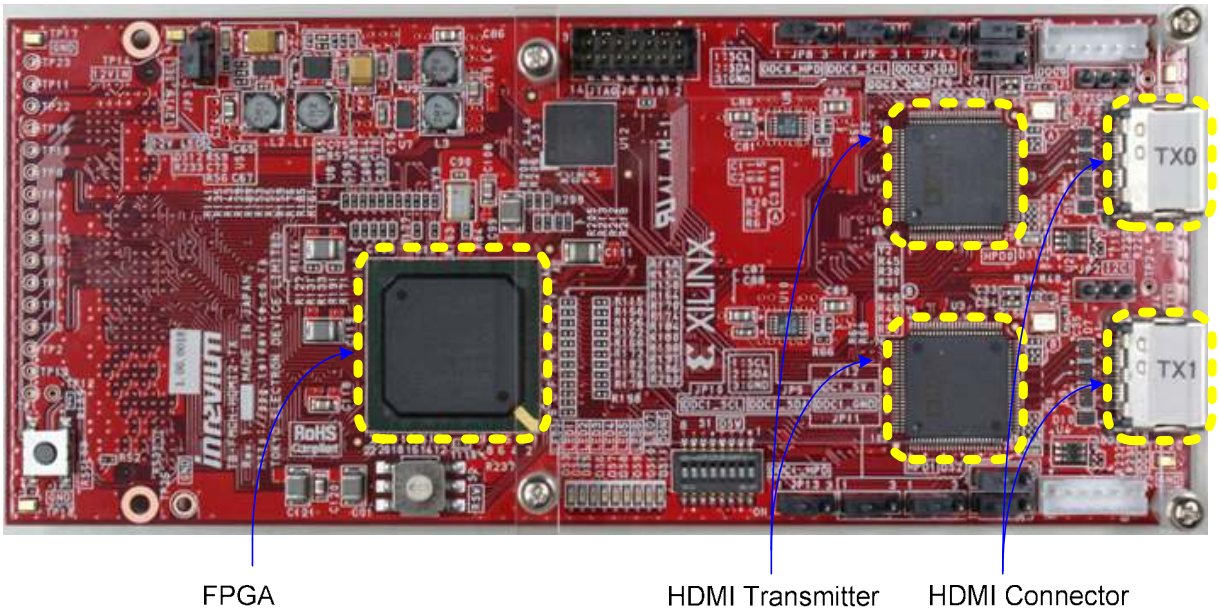

Figure 5-2 TB-FMCH-HDMI2-TX (component side)

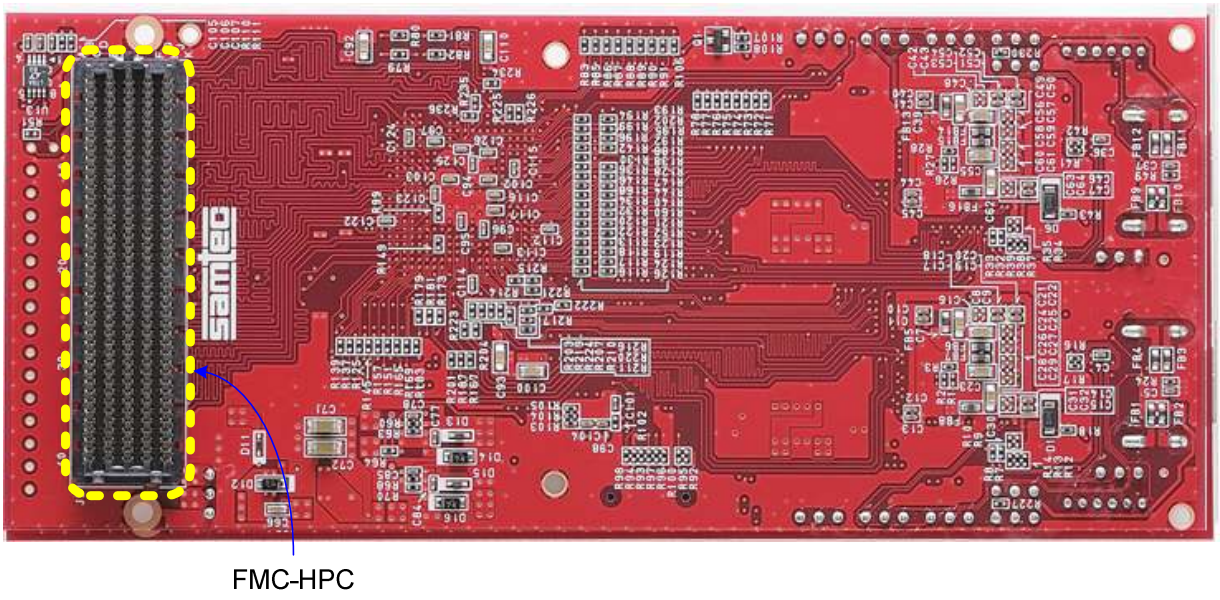

Figure 5-3 TB-FMCH-HDMI2-TX (solder side)

5.3. Board Specification

Figure 5-4 shows the TB-FMCH-HDMI2-TX board specification.

External Dimensions	: W:160mm x H:69mm
Number of Layers	: 8 Layers
Board Thickness	: 1.6 mm
Material	: FR-4
FPGA	: Xilinx's XC6SLX45-3FGG484C
FMC Connector	: Samtec's ASP-134488-01
HDMI Connector	: Molex's 5002541927

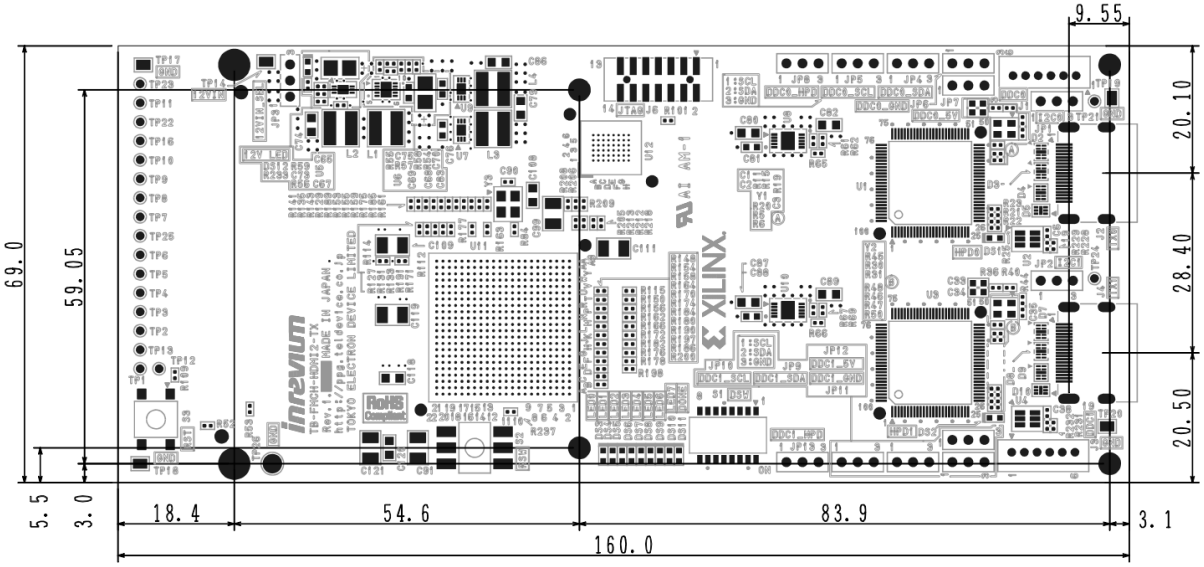

Figure 5-4 TB-FMCH-HDMI2-TX Board Dimensions

5.4. Power Supply to the Board

Figure 5-5 shows the TB-FMCH-HDMI2-TX power supply structure.

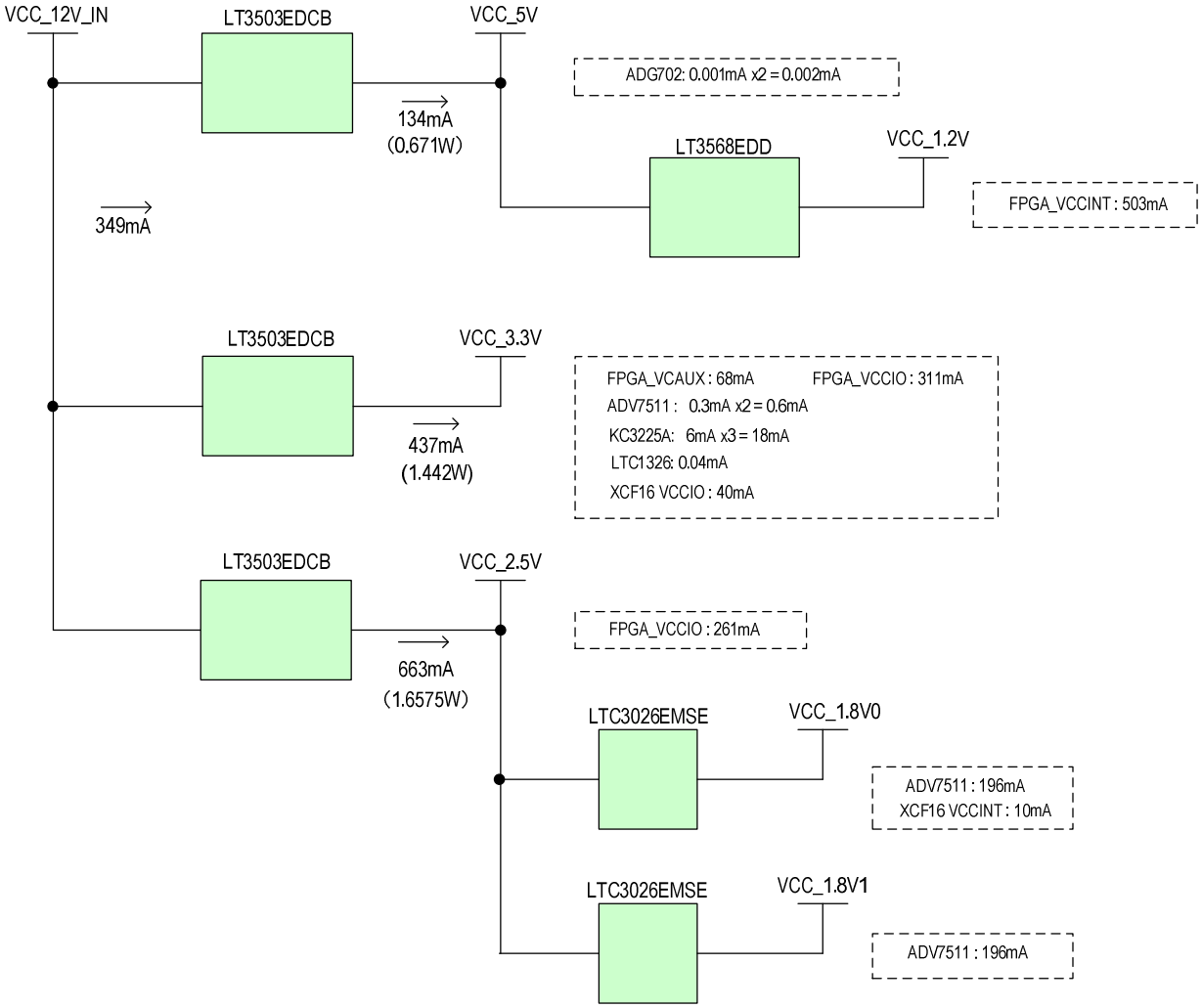

Figure 5-5 TB-FMCH-HDMI2-TX Power Supply Structure

5.5. HDMI Transmitter

The HDMI connector uses MOLEX's 5002541927.
The HDMI transmitter uses Analog Devices's ADV7511KSTZ-P.
The following device is used for ESD protection:
ESD protection: Semtech's RCLAMP0524 and RCLAMP0504
Table 5-1 shows the HDMI connector pin assignment.

Table 5-1 HDMI Connector (transmit side)

Pin #	Name	Description
1	TMDS DATA2+	TMDS Transmit Data 2+
2	TMDS SHLD2	TMDS Transmit Data 2 Shield
3	TMDS DATA2-	TMDS Transmit Data 2-
4	TMDS DATA1+	TMDS Transmit Data 1+
5	TMDS SHLD1	TMDS Transmit Data 1 Shield
6	TMDS DATA1-	TMDS Transmit Data 1-
7	TMDS DATA0+	TMDS Transmit Data 0+
8	TMDS SHLD0	TMDS Transmit Data 0 Shield
9	TMDS DATA0-	TMDS Transmit Data 0-
10	TMDS CLK+	TMDS Transmit Clock+
11	TMDS CLK SHLD	TMDS Transmit Clock Shield
12	TMDS CLK-	TMDS Transmit Clock-
13	CEC	CEC Signal
14	UTILITY/HEAC+	HEAC+ Signal
15	DDC_SCL	DDC Serial Clock
16	DDC_SDA	DDC Serial Data
17	DDC/CEC GND	DDC/CEC Ground
18	DDC_+5V	+5V
19	HPD/HEAC-	Hot Plug Detection/HEAC-Signal

5.6. FMC Connector

The FMC connector connecting to the High-Pin Count uses SAMTEC's ASP-134488-01.
Power to the TB-FMCH-HDMI2-TX is supplied from a +12V on the main board.
An external power source can also be used.
Table 5-2 shows JP3 jumper setting for power supply.

Table 5-2 JP3 Jumper Setting

No	Purpose	Silk	Jumper Setting
1	FMC Connector	12VIN_SEL	JP3: 1-2 short
2	External Power Source	12VIN_SEL	JP3: 2-3 short

The following test pin is used to connect an external power source.
TP14: 12VIN

Table 5-3 shows the FMC connector pin assignment.

Table 5-3 FMC Connector Pin Assignment

Pin	A-row	B-row	C-row	D-row	E-row
1	GND	RES1	GND	PG_C2M	GND
2	DP1_M2C_P	GND	DP0_C2M_P	GND	HA01_P_CC
3	DP1_M2C_N	GND	DP0_C2M_N	GND	HA01_N_CC
4	GND	DP9_M2C_P	GND	GBTCLK0_M2C_P	GND
5	GND	DP9_M2C_N	GND	GBTCLK0_M2C_N	GND
6	DP2_M2C_P	GND	DP0_M2C_P	GND	HA05_P
7	DP2_M2C_N	GND	DP0_M2C_N	GND	HA05_N
8	GND	DP8_M2C_P	GND	LA01_P_CC	GND
9	GND	DP8_M2C_N	GND	LA01_N_CC	HA09_P
10	DP3_M2C_P	GND	LA06_P	GND	HA09_N
11	DP3_M2C_N	GND	LA06_N	LA05_P	GND
12	GND	DP7_M2C_P	GND	LA05_N	HA13_P
13	GND	DP7_M2C_N	GND	GND	HA13_N
14	DP4_M2C_P	GND	LA10_P	LA09_P	GND
15	DP4_M2C_N	GND	LA10_N	LA09_N	HA16_P
16	GND	DP6_M2C_P	GND	GND	HA16_N
17	GND	DP6_M2C_N	GND	LA13_P	GND
18	DP5_M2C_P	GND	LA14_P	LA13_N	HA20_P
19	DP5_M2C_N	GND	LA14_N	GND	HA20_N
20	GND	GBTCLK1_M2C_P	GND	LA17_P_CC	GND
21	GND	GBTCLK1_M2C_N	GND	LA17_N_CC	HB03_P
22	DP1_C2M_P	GND	LA18_P_CC	GND	HB03_N
23	DP1_C2M_N	GND	LA18_N_CC	LA23_P	GND
24	GND	DP2_C9M_P	GND	LA23_N	HB05_P
25	GND	DP2_C9M_N	GND	GND	HB05_N
26	DP2_C2M_P	GND	LA27_P	LA26_P	GND
27	DP2_C2M_N	GND	LA27_N	LA26_N	HB09_P
28	GND	DP2_C8M_P	GND	GND	HB09_N
29	GND	DP2_C8M_N	GND	TCK	GND
30	DP3_C2M_P	GND	SCL	TDI	HB13_P
31	DP3_C2M_N	GND	SDA	TDO	HB13_N
32	GND	DP2_C7M_P	GND	+3.3VAUX	GND
33	GND	DP2_C7M_N	GND	TMS	HB19_P
34	DP4_C2M_P	GND	GA0	TRST	HB19_N
35	DP4_C2M_N	GND	+12V	GA1	GND
36	GND	DP2_C6M_P	GND	+3.3V	HB21_P
37	GND	DP2_C6M_N	+12V	GND	HB21_N
38	DP5_C2M_P	GND	GND	+3.3V	GND
39	DP5_C2M_N	GND	+3.3V	GND	VADJ
40	GND	RES0	GND	+3.3V	GND

Pin	F-row	G-row	H-row	J-row	K-row
1	PG_M2C	GND	VREF_A_M2C	GND	VREF_B_M2C
2	GND	CLK1_M2C_P	PRSNT_M2C_L	CLK3_M2C_P	GND
3	GND	CLK1_M2C_N	GND	CLK3_M2C_N	GND
4	HA00_P_CC	GND	CLK0_M2C_P	GND	CLK2_M2C_P
5	HA00_N_CC	GND	CLK0_M2C_N	GND	CLK2_M2C_N
6	GND	LA00_P_CC	GND	HA03_P	GND
7	GND	LA00_N_CC	LA02_P	HA03_N	HA02_P
8	HA04_P	GND	LA02_N	GND	HA02_N
9	HA04_N	LA03_P	GND	HA07_P	GND
10	GND	LA03_N	LA04_P	HA07_N	HA06_P
11	HA08_P	GND	LA04_N	GND	HA06_N
12	HA08_N	LA08_P	GND	HA11_P	GND
13	GND	LA08_N	LA07_P	HA11_N	HA10_P
14	HA12_P	GND	LA07_N	GND	HA10_N
15	HA12_N	LA12_P	GND	HA14_P	GND
16	GND	LA12_N	LA11_P	HA14_N	HA17_P_CC
17	HA15_P	GND	LA11_N	GND	HA17_N_CC
18	HA15_N	LA16_P	GND	HA18_P	GND
19	GND	LA16_N	LA15_P	HA18_N	HA21_P
20	HA19_P	GND	LA15_N	GND	HA21_N
21	HA19_N	LA20_P	GND	HA22_P	GND
22	GND	LA20_N	LA19_P	HA22_N	HA23_P
23	HB02_P	GND	LA19_N	GND	HA23_N
24	HB02_N	LA22_P	GND	HB01_P	GND
25	GND	LA22_N	LA21_P	HB01_N	HB00_P_CC
26	HB04_P	GND	LA21_N	GND	HB00_N_CC
27	HB04_N	LA25_P	GND	HB07_P	GND
28	GND	LA25_N	LA24_P	HB07_N	HB06_P_CC
29	HB08_P	GND	LA24_N	GND	HB06_N_CC
30	HB08_N	LA29_P	GND	HB11_P	GND
31	GND	LA29_N	LA28_P	HB11_N	HB10_P
32	HB12_P	GND	LA28_N	GND	HB10_N
33	HB12_N	LA31_P	GND	HB15_P	GND
34	GND	LA31_N	LA30_P	HB15_N	HB14_P
35	HB16_P	GND	LA30_N	GND	HB14_N
36	HB16_N	LA33_P	GND	HB18_P	GND
37	GND	LA33_N	LA32_P	HB18_N	HB17_P_CC
38	HB20_P	GND	LA32_N	GND	HB17_N_CC
39	HB20_N	VADJ	GND	VIO_B_M2C	GND
40	VADJ	GND	VADJ	GND	VIO_B_M2C

5.7. Other Interfaces

The board also provides the following interfaces.

5.7.1. JTAG Interface

The board has a JTAG connector FPGA configuration.

JTAG Connector: Molex's 87832-1420

Table 5-4 JTAG Connector

Pin	Signal	Pin	Signal Name
1	GND	2	3.3V
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	NC
13	GND	14	NC

5.7.2. General-Purpose Clock Interface

The board has a general-purpose clock on FPGA (27MHz crystal oscillator)

KC5032C027.0000C30E00 (Kyocera)

5.8. LED Status

Table 5-5 shows the onboard LED function.

Table 5-5 LED Status

No	Circuit #	Silk	Purpose	Description
1	DS3	LED0	General-purpose LED0	[TX0]I2C config state Off: CFG done / On: CFG active
2	DS4	LED1	General-purpose LED1	[TX0]I2C read back Off: Error / On: No error
3	DS5	LED2	General-purpose LED2	[TX0]Video status LED2: OFF, LED3: OFF : 2D Video LED2: ON, LED3: OFF : 3D SideBySide LED2: OFF, LED3: ON : 3D TopAndBottom LED2: ON, LED3: ON : 3D FramePacking
4	DS6	LED3	General-purpose LED3	
5	DS7	LED4	General-purpose LED4	Unused (On)
6	DS8	LED5	General-purpose LED5	[TX0] input video image clock monitor Flashing: Active clock / Off: No clock
7	DS9	LED6	General-purpose LED6	[TX1] input video image clock monitor Flashing: Active clock / Off: No clock
8	DS10	LED7	General-purpose LED7	System Reset Monitor On: Reset active / Off: Reset release
9	DS1	HPD0	TX0 hot plug display	On: Connected state
10	DS2	HPD1	TX1 hot plug display	On: Connected state
11	DS11	DONE	Config display	On: Config complete
12	DS12	12VLED	12V display	On: 12V active

5.9. Control Function

Table 5-6 shows the onboard switch function.

Table 5-6 Switch Function

No	Circuit #	Silk	Description
1	S1-1	DSW	ADV7511 config ROM selection: *Please see Table 5-7.
2	S1-2	DSW	
3	S1-3	DSW	
4	S1-4	DSW	
5	S1-5	DSW	Unused *set to ON.
6	S1-6	DSW	Unused *set to ON.
7	S1-7	DSW	Unused *set to ON.
8	S1-8	DSW	Unused *set to ON.
9	S2	RSW	Unused *set to '0'.
10	S3	RST	FPGA reconfig (long push – 3 seconds) FPGA reset (short push)

5.9.1. ADV7511 Configuration ROM selection

Table 5-7 shows the configuration ROM function and settings for ADV7511.

Table 5-7 ADV7511 configuration ROM

No	DSW (S1-4)	DSW (S1-3)	DSW (S1-2)	DSW (S1-1)	Color format
1	ON	ON	ON	ON	Color Space:YCbCr 444, Color Depth:8bit
2	ON	ON	ON	OFF	Color Space:YCbCr 444, Color Depth:10bit
3	ON	ON	OFF	ON	Color Space:YCbCr 444, Color Depth:12bit
4	ON	ON	OFF	OFF	-
5	ON	OFF	ON	ON	Color Space:YCbCr 422, Color Depth:8bit
6	ON	OFF	ON	OFF	Color Space:YCbCr 422, Color Depth:10bit
7	ON	OFF	OFF	ON	Color Space:YCbCr 422, Color Depth:12bit
8	ON	OFF	OFF	OFF	-
9	OFF	ON	ON	ON	Color Space:RGB, Color Depth:8bit
10	OFF	ON	ON	OFF	Color Space:RGB, Color Depth:10bit
11	OFF	ON	OFF	ON	Color Space:RGB, Color Depth:12bit
12	OFF	ON	OFF	OFF	-
13	OFF	OFF	ON	ON	-
14	OFF	OFF	ON	OFF	-
15	OFF	OFF	OFF	ON	-
16	OFF	OFF	OFF	OFF	-

5.10. FPGA Pin Assignment

Table 5-8 shows the FPGA pin assignment.

In case of 8-bit signal format, active bits are assigned to MSB 8-bit of each RGB pin of FMC. LSB 2-bit are always 2'b00 in 8-bit signal format.

Table 5-8 FPGA Pin Assignment

Pin Name	No.	IO	Spec.	Description
CLK0_M2C_P	B10	I	LVCMOS25	TX#0_DCLK Signal (FMC to FPGA)
CLK1_M2C_P	C11	IO	LVCMOS25	Unused
LA00_P_CC	D6	I	LVCMOS25	TX#0_VSYNC Signal (FMC to FPGA)
LA01_P_CC	C7	I	LVCMOS25	TX#0_HSYNC Signal (FMC to FPGA)
LA02_P	D9	I	LVCMOS25	TX#0_DE Signal (FMC to FPGA)
LA03_P	D7	I	LVCMOS25	TX#0_D0 Signal (FMC to FPGA) [Cb0/B0]
LA04_P	C13	I	LVCMOS25	TX#0_D1 Signal (FMC to FPGA) [Cb1/B1]
LA05_P	B14	I	LVCMOS25	TX#0_D2 Signal (FMC to FPGA) [Cb2/B2]
LA06_P	D15	I	LVCMOS25	TX#0_D3 Signal (FMC to FPGA) [Cb3/B3]
LA07_P	C17	I	LVCMOS25	TX#0_D4 Signal (FMC to FPGA) [Cb4/B4]
LA08_P	E16	I	LVCMOS25	TX#0_D5 Signal (FMC to FPGA) [Cb5/B5]
LA09_P	G16	I	LVCMOS25	TX#0_D6 Signal (FMC to FPGA) [Cb6/B6]
LA10_P	B21	I	LVCMOS25	TX#0_D7 Signal (FMC to FPGA) [Cb7/B7]
LA11_P	K16	I	LVCMOS25	TX#0_D8 Signal (FMC to FPGA) [Cb8/B8]
LA12_P	D19	I	LVCMOS25	TX#0_D9 Signal (FMC to FPGA) [Cb9/B9]
LA13_P	D21	I	LVCMOS25	TX#0_D10 Signal (FMC to FPGA) [Cb10/B10]
LA14_P	G19	I	LVCMOS25	TX#0_D11 Signal (FMC to FPGA) [Cb11/B11]
LA15_P	E20	I	LVCMOS25	TX#0_D12 Signal (FMC to FPGA) [Y0/G0]
LA16_P	F21	I	LVCMOS25	TX#0_D13 Signal (FMC to FPGA) [Y1/G1]
LA17_P_CC	G20	I	LVCMOS25	TX#0_D14 Signal (FMC to FPGA) [Y2/G2]
LA18_P_CC	H21	I	LVCMOS25	TX#0_D15 Signal (FMC to FPGA) [Y3/G3]
LA19_P	J20	I	LVCMOS25	TX#0_D16 Signal (FMC to FPGA) [Y4/G4]
LA20_P	L20	I	LVCMOS25	TX#0_D17 Signal (FMC to FPGA) [Y5/G5]
LA21_P	N20	I	LVCMOS25	TX#0_D18 Signal (FMC to FPGA) [Y6/G6]
LA22_P	R20	I	LVCMOS25	TX#0_D19 Signal (FMC to FPGA) [Y7/G7]
LA23_P	U20	I	LVCMOS25	TX#0_D20 Signal (FMC to FPGA) [Y8/G8]
LA24_P	M19	I	LVCMOS25	TX#0_D21 Signal (FMC to FPGA) [Y9/G9]
LA25_P	M16	I	LVCMOS25	TX#0_D22 Signal (FMC to FPGA) [Y10/G10]
LA26_P	P19	I	LVCMOS25	TX#0_D23 Signal (FMC to FPGA) [Y11/G11]
LA27_P	W20	I	LVCMOS25	TX#0_D24 Signal (FMC to FPGA) [Cr0/R0]
LA28_P	L17	I	LVCMOS25	TX#0_D25 Signal (FMC to FPGA) [Cr1/R1]
LA29_P	U19	I	LVCMOS25	TX#0_D26 Signal (FMC to FPGA) [Cr2/R2]
LA30_P	M17	I	LVCMOS25	TX#0_D27 Signal (FMC to FPGA) [Cr3/R3]
LA31_P	P17	I	LVCMOS25	TX#0_D28 Signal (FMC to FPGA) [Cr4/R4]
LA32_P	P18	I	LVCMOS25	TX#0_D29 Signal (FMC to FPGA) [Cr5/R5]
LA33_P	T19	IO	LVCMOS25	Unused
CLK0_M2C_N	A10	I	LVCMOS25	Unused
CLK1_M2C_N	A11	IO	LVCMOS25	Unused

Pin Name	No.	IO	Spec.	Description
LA00_N_CC	C6	I	LVCMOS25	TX#0_input video status[0] (FPGA to FMC)
LA01_N_CC	A7	I	LVCMOS25	TX#0_input video status[1] (FPGA to FMC) *Please see Note
LA02_N	C8	I	LVCMOS25	Unused
LA03_N	D8	I	LVCMOS25	Unused
LA04_N	A13	I	LVCMOS25	Unused
LA05_N	A14	I	LVCMOS25	Unused
LA06_N	C16	I	LVCMOS25	Unused
LA07_N	A17	I	LVCMOS25	Unused
LA08_N	D17	I	LVCMOS25	Unused
LA09_N	G17	I	LVCMOS25	Unused
LA10_N	B22	I	LVCMOS25	Unused
LA11_N	J16	I	LVCMOS25	Unused
LA12_N	D20	I	LVCMOS25	Unused
LA13_N	D22	I	LVCMOS25	Unused
LA14_N	F20	I	LVCMOS25	Unused
LA15_N	E22	I	LVCMOS25	Unused
LA16_N	F22	I	LVCMOS25	Unused
LA17_N_CC	G22	I	LVCMOS25	Unused
LA18_N_CC	H22	I	LVCMOS25	Unused
LA19_N	J22	I	LVCMOS25	TX#0_MCLK signal (FMC to FPGA)
LA20_N	L22	I	LVCMOS25	TX#0_SCLK signal (FMC to FPGA)
LA21_N	N22	I	LVCMOS25	TX#0_AP0 signal (FMC to FPGA)
LA22_N	R22	I	LVCMOS25	TX#0_AP1 signal (FMC to FPGA)
LA23_N	U22	I	LVCMOS25	TX#0_AP2 signal (FMC to FPGA)
LA24_N	N19	I	LVCMOS25	TX#0_AP3 signal (FMC to FPGA)
LA25_N	L15	I	LVCMOS25	TX#0_AP4 signal (FMC to FPGA)
LA26_N	P20	I	LVCMOS25	TX#0_AP5 signal (FMC to FPGA)
LA27_N	W22	I	LVCMOS25	TX#0_P30 signal (FMC to FPGA) [Cr6/R6]
LA28_N	K18	I	LVCMOS25	TX#0_P31 signal (FMC to FPGA) [Cr7/R7]
LA29_N	V20	I	LVCMOS25	TX#0_P32 signal (FMC to FPGA) [Cr8/R8]
LA30_N	M18	I	LVCMOS25	TX#0_P33 signal (FMC to FPGA) [Cr9/R9]
LA31_N	N16	I	LVCMOS25	TX#0_P34 signal (FMC to FPGA) [Cr10/R10]
LA32_N	R19	I	LVCMOS25	TX#0_P35 signal (FMC to FPGA) [Cr11/R11]
LA33_N	T20	IO	LVCMOS25	Unused
CLK2_M2C_P	D11	IO	LVCMOS25	Unused
CLK3_M2C_P	B12	IO	LVCMOS25	Unused
HA00_P_CC	B6	IO	LVCMOS25	Unused
HA01_P_CC	B8	IO	LVCMOS25	Unused
HA02_P	C9	IO	LVCMOS25	Unused
HA03_P	D10	IO	LVCMOS25	Unused
HA04_P	D14	IO	LVCMOS25	Unused
HA05_P	C15	IO	LVCMOS25	Unused

Pin Name	No.	IO	Spec.	Description
HA06_P	B16	IO	LVCMOS25	Unused
HA07_P	B18	IO	LVCMOS25	Unused
HA08_P	C19	IO	LVCMOS25	Unused
HA09_P	F16	IO	LVCMOS25	Unused
HA10_P	A20	IO	LVCMOS25	Unused
HA11_P	H16	IO	LVCMOS25	Unused
HA12_P	F18	IO	LVCMOS25	Unused
HA13_P	C20	IO	LVCMOS25	Unused
HA14_P	H19	IO	LVCMOS25	Unused
HA15_P	J17	IO	LVCMOS25	Unused
HA16_P	H20	IO	LVCMOS25	Unused
HA17_P_CC	K20	IO	LVCMOS25	Unused
HA18_P	M20	IO	LVCMOS25	Unused
HA19_P	K21	IO	LVCMOS25	Unused
HA20_P	M21	IO	LVCMOS25	Unused
HA21_P	P21	IO	LVCMOS25	Unused
HA22_P	T21	IO	LVCMOS25	Unused
HA23_P	V21	IO	LVCMOS25	Unused
CLK2_M2C_N	C12	IO	LVCMOS25	Unused
CLK3_M2C_N	A12	IO	LVCMOS25	Unused
HA00_N_CC	A6	IO	LVCMOS25	Unused
HA01_N_CC	A8	IO	LVCMOS25	Unused
HA02_N	A9	IO	LVCMOS25	Unused
HA03_N	C10	IO	LVCMOS25	Unused
HA04_N	C14	IO	LVCMOS25	Unused
HA05_N	A15	IO	LVCMOS25	Unused
HA06_N	A16	IO	LVCMOS25	Unused
HA07_N	A18	IO	LVCMOS25	Unused
HA08_N	B20	IO	LVCMOS25	Unused
HA09_N	F17	IO	LVCMOS25	Unused
HA10_N	A21	IO	LVCMOS25	Unused
HA11_N	H17	IO	LVCMOS25	Unused
HA12_N	F19	IO	LVCMOS25	Unused
HA13_N	C22	IO	LVCMOS25	Unused
HA14_N	H18	IO	LVCMOS25	Unused
HA15_N	K17	IO	LVCMOS25	Unused
HA16_N	J19	IO	LVCMOS25	Unused
HA17_N_CC	K19	IO	LVCMOS25	Unused
HA18_N	L19	IO	LVCMOS25	Unused
HA19_N	K22	IO	LVCMOS25	Unused
HA20_N	M22	IO	LVCMOS25	Unused
HA21_N	P22	IO	LVCMOS25	Unused

Pin Name	No.	IO	Spec.	Description
HA22_N	T22	IO	LVCMOS25	Unused
HA23_N	V22	IO	LVCMOS25	Unused
TX#0_D35	Y18	O	LVCMOS33	TX#0 Video data 35 (FPGA to TX)
TX#0_D34	T16	O	LVCMOS33	TX#0 Video data 34 (FPGA to TX)
TX#0_D33	T15	O	LVCMOS33	TX#0 Video data 33 (FPGA to TX)
TX#0_D32	U17	O	LVCMOS33	TX#0 Video data 32 (FPGA to TX)
TX#0_D31	U16	O	LVCMOS33	TX#0 Video data 31 (FPGA to TX)
TX#0_D30	V19	O	LVCMOS33	TX#0 Video data 30 (FPGA to TX)
TX#0_D29	V18	O	LVCMOS33	TX#0 Video data 29 (FPGA to TX)
TX#0_D28	R16	O	LVCMOS33	TX#0 Video data 28 (FPGA to TX)
TX#0_D27	R15	O	LVCMOS33	TX#0 Video data 27 (FPGA to TX)
TX#0_D26	V17	O	LVCMOS33	TX#0 Video data 26 (FPGA to TX)
TX#0_D25	W17	O	LVCMOS33	TX#0 Video data 25 (FPGA to TX)
TX#0_D24	V15	O	LVCMOS33	TX#0 Video data 24 (FPGA to TX)
TX#0_D23	AA18	O	LVCMOS33	TX#0 Video data 23 (FPGA to TX)
TX#0_D22	AB18	O	LVCMOS33	TX#0 Video data 22 (FPGA to TX)
TX#0_D21	Y17	O	LVCMOS33	TX#0 Video data 21 (FPGA to TX)
TX#0_D20	AB17	O	LVCMOS33	TX#0 Video data 20 (FPGA to TX)
TX#0_D19	AA14	O	LVCMOS33	TX#0 Video data 19 (FPGA to TX)
TX#0_D18	AB14	O	LVCMOS33	TX#0 Video data 18 (FPGA to TX)
TX#0_D17	Y16	O	LVCMOS33	TX#0 Video data 17 (FPGA to TX)
TX#0_D16	W15	O	LVCMOS33	TX#0 Video data 16 (FPGA to TX)
TX#0_D15	V13	O	LVCMOS33	TX#0 Video data 15 (FPGA to TX)
TX#0_D14	W13	O	LVCMOS33	TX#0 Video data 14 (FPGA to TX)
TX#0_D13	AA16	O	LVCMOS33	TX#0 Video data 13 (FPGA to TX)
TX#0_D12	AB16	O	LVCMOS33	TX#0 Video data 12 (FPGA to TX)
TX#0_D11	W14	O	LVCMOS33	TX#0 Video data 11 (FPGA to TX)
TX#0_D10	Y14	O	LVCMOS33	TX#0 Video data 10 (FPGA to TX)
TX#0_D9	Y15	O	LVCMOS33	TX#0 Video data 9 (FPGA to TX)
TX#0_D8	AB15	O	LVCMOS33	TX#0 Video data 8 (FPGA to TX)
TX#0_D7	T12	O	LVCMOS33	TX#0 Video data 7 (FPGA to TX)
TX#0_D6	U12	O	LVCMOS33	TX#0 Video data 6 (FPGA to TX)
TX#0_D5	T14	O	LVCMOS33	TX#0 Video data 5 (FPGA to TX)
TX#0_D4	R13	O	LVCMOS33	TX#0 Video data 4 (FPGA to TX)
TX#0_D3	R11	O	LVCMOS33	TX#0 Video data 3 (FPGA to TX)
TX#0_D2	T11	O	LVCMOS33	TX#0 Video data 2 (FPGA to TX)
TX#0_D1	AA10	O	LVCMOS33	TX#0 Video data 1 (FPGA to TX)
TX#0_D0	AB10	O	LVCMOS33	TX#0 Video data 0 (FPGA to TX)
TX#0_DCLK	W12	O	LVCMOS33	TX#0 DCLK signal (FPGA to TX)
SYSCLK_P	Y11	I	LVCMOS33	System clock (27MHz)
TX#0_DE	W11	O	LVCMOS33	TX#0 data enable (FPGA to TX)
TX#0_HSYNC	Y9	O	LVCMOS33	TX#0 HSYNC (FPGA to TX)

Pin Name	No.	IO	Spec.	Description
TX#0_VSYNC	AB9	O	LVCMOS33	TX#0 VSYNC (FPGA to TX)
TX#0_DSD0	W10	O	LVCMOS33	TX#0 DSD Audio data 0 (FPGA to TX)
TX#0_DSD1	Y10	O	LVCMOS33	TX#0 DSD Audio data 1 (FPGA to TX)
TX#0_DSD2	AA8	O	LVCMOS33	TX#0 DSD Audio data 2 (FPGA to TX)
TX#0_DSD3	AB8	O	LVCMOS33	TX#0 DSD Audio data 3 (FPGA to TX)
TX#0_DSD4	W8	O	LVCMOS33	TX#0 DSD Audio data 4 (FPGA to TX)
TX#0_DSD5	V7	O	LVCMOS33	TX#0 DSD Audio data 5 (FPGA to TX)
TX#0_DSD_CLK	W9	O	LVCMOS33	TX#0 DSD clock (FPGA to TX)
TX#0_SPDIF	Y8	O	LVCMOS33	TX#0 SPDIF Digital Audio (FPGA to TX)
TX#0_MCLK	AB7	O	LVCMOS33	TX#0 Audio Master Clock (FPGA to TX)
TX#0_I2S0	U9	O	LVCMOS33	TX#0 I2S Audio Signal 0 (FPGA to TX)
TX#0_I2S1	V9	O	LVCMOS33	TX#0 I2S Audio Signal 1 (FPGA to TX)
TX#0_I2S2	T8	O	LVCMOS33	TX#0 I2S Audio Signal 2 (FPGA to TX)
TX#0_I2S3	U8	O	LVCMOS33	TX#0 I2S Audio Signal 3 (FPGA to TX)
TX#0_SCLK	T10	O	LVCMOS33	TX#0 Audio Serial Clock (FPGA to TX)
TX#0_LRCLK	U10	O	LVCMOS33	TX#0 LRCLK Signal (FPGA to TX)
TX#0_HPD_IO	W6	O	LVCMOS33	TX#0 Hot Plug Control (FPGA to TX)
TX#0_PD	T18	O	LVCMOS33	TX#0 Power Down (FPGA to TX)
TX#0_INT	Y19	I	LVCMOS33	TX#0 Interrupt (TX to FPGA)
TX#0_SCL	AB19	O	LVCMOS33	TX#0 Serial Clock (FPGA to TX)
TX#0_SDA	W18	IO	LVCMOS33	TX#0 Serial Data (FPGA to TX)
FPGA_SRSTN	AA2	O	LVCMOS33	FPGA Reset
TX#1_D35	W3	O	LVCMOS33	TX#1 Video data 35 (FPGA to TX)
TX#1_D34	W1	O	LVCMOS33	TX#1 Video data 34 (FPGA to TX)
TX#1_D33	P8	O	LVCMOS33	TX#1 Video data 33 (FPGA to TX)
TX#1_D32	P7	O	LVCMOS33	TX#1 Video data 32 (FPGA to TX)
TX#1_D31	P6	O	LVCMOS33	TX#1 Video data 31 (FPGA to TX)
TX#1_D30	P5	O	LVCMOS33	TX#1 Video data 30 (FPGA to TX)
TX#1_D29	T4	O	LVCMOS33	TX#1 Video data 29 (FPGA to TX)
TX#1_D28	T3	O	LVCMOS33	TX#1 Video data 28 (FPGA to TX)
TX#1_D27	U4	O	LVCMOS33	TX#1 Video data 27 (FPGA to TX)
TX#1_D26	V3	O	LVCMOS33	TX#1 Video data 26 (FPGA to TX)
TX#1_D25	N6	O	LVCMOS33	TX#1 Video data 25 (FPGA to TX)
TX#1_D24	N7	O	LVCMOS33	TX#1 Video data 24 (FPGA to TX)
TX#1_D23	M7	O	LVCMOS33	TX#1 Video data 23 (FPGA to TX)
TX#1_D22	M8	O	LVCMOS33	TX#1 Video data 22 (FPGA to TX)
TX#1_D21	R4	O	LVCMOS33	TX#1 Video data 21 (FPGA to TX)
TX#1_D20	P4	O	LVCMOS33	TX#1 Video data 20 (FPGA to TX)
TX#1_D19	M6	O	LVCMOS33	TX#1 Video data 19 (FPGA to TX)
TX#1_D18	L6	O	LVCMOS33	TX#1 Video data 18 (FPGA to TX)
TX#1_D17	P3	O	LVCMOS33	TX#1 Video data 17 (FPGA to TX)
TX#1_D16	N4	O	LVCMOS33	TX#1 Video data 16 (FPGA to TX)

Pin Name	No.	IO	Spec.	Description
TX#1_D15	M5	O	LVCMOS33	TX#1 Video data 15 (FPGA to TX)
TX#1_D14	M4	O	LVCMOS33	TX#1 Video data 14 (FPGA to TX)
TX#1_D13	V2	O	LVCMOS33	TX#1 Video data 13 (FPGA to TX)
TX#1_D12	V1	O	LVCMOS33	TX#1 Video data 12 (FPGA to TX)
TX#1_D11	U3	O	LVCMOS33	TX#1 Video data 11 (FPGA to TX)
TX#1_D10	U1	O	LVCMOS33	TX#1 Video data 10 (FPGA to TX)
TX#1_D9	T2	O	LVCMOS33	TX#1 Video data 9 (FPGA to TX)
TX#1_D8	T1	O	LVCMOS33	TX#1 Video data 8 (FPGA to TX)
TX#1_D7	R3	O	LVCMOS33	TX#1 Video data 7 (FPGA to TX)
TX#1_D6	R1	O	LVCMOS33	TX#1 Video data 6 (FPGA to TX)
TX#1_D5	P2	O	LVCMOS33	TX#1 Video data 5 (FPGA to TX)
TX#1_D4	P1	O	LVCMOS33	TX#1 Video data 4 (FPGA to TX)
TX#1_D3	N3	O	LVCMOS33	TX#1 Video data 3 (FPGA to TX)
TX#1_D2	N1	O	LVCMOS33	TX#1 Video data 2 (FPGA to TX)
TX#1_D1	M2	O	LVCMOS33	TX#1 Video data 1 (FPGA to TX)
TX#1_D0	M1	O	LVCMOS33	TX#1 Video data 0 (FPGA to TX)
TX#1_DCLK	J3	O	LVCMOS33	TX#1 DCLK signal (FPGA to TX)
TX#1_DE	L1	O	LVCMOS33	TX#1 data enable (FPGA to TX)
TX#1_HSYNC	K2	O	LVCMOS33	TX#1 HSYNC (FPGA to TX)
TX#1_VSYNC	K1	O	LVCMOS33	TX#1 VSYNC (FPGA to TX)
TX#1_DSD0	M3	O	LVCMOS33	TX#1 DSD Audio data 0 (FPGA to TX)
TX#1_DSD1	L4	O	LVCMOS33	TX#1 DSD Audio data 1 (FPGA to TX)
TX#1_DSD2	K5	O	LVCMOS33	TX#1 DSD Audio data 2 (FPGA to TX)
TX#1_DSD3	K4	O	LVCMOS33	TX#1 DSD Audio data 3 (FPGA to TX)
TX#1_DSD4	K3	O	LVCMOS33	TX#1 DSD Audio data 4 (FPGA to TX)
TX#1_DSD5	J4	O	LVCMOS33	TX#1 DSD Audio data 5 (FPGA to TX)
TX#1_DSD_CLK	K6	O	LVCMOS33	TX#1 DSD clock (FPGA to TX)
TX#1_SPDIF	J6	O	LVCMOS33	TX#1 SPDIF Digital Audio (FPGA to TX)
TX#1_MCLK	H4	O	LVCMOS33	TX#1 Audio Master Clock (FPGA to TX)
TX#1_I2S0	H3	O	LVCMOS33	TX#1 I2S Audio signal 0 (FPGA to TX)
TX#1_I2S1	H2	O	LVCMOS33	TX#1 I2S Audio signal 1 (FPGA to TX)
TX#1_I2S2	H1	O	LVCMOS33	TX#1 I2S Audio signal 2 (FPGA to TX)
TX#1_I2S3	G3	O	LVCMOS33	TX#1 I2S Audio signal 3 (FPGA to TX)
TX#1_SCLK	G1	O	LVCMOS33	TX#1 Audio serial clock (FPGA to TX)
TX#1_LRCLK	H6	O	LVCMOS33	TX#1 LRCLK signal (FPGA to TX)
TX#1_HPD_IO	H5	O	LVCMOS33	TX#1 hot plug control (FPGA to TX)
TX#1_PD	G4	O	LVCMOS33	TX#1 power down (FPGA to TX)
TX#1_INT	F2	I	LVCMOS33	TX#1 interrupt (TX to FPGA)
TX#1_SCL	Y2	O	LVCMOS33	TX#1 serial clock (FPGA to TX)
TX#1_SDA	Y1	IO	LVCMOS33	TX#1 serial data (FPGA to/from TX)
RSW0	D2	I	LVCMOS33	Rotary switch 0
RSW1	D1	I	LVCMOS33	Rotary switch 1

Pin Name	No.	IO	Spec.	Description
RSW2	C3	I	LVCMOS33	Rotary switch 2
RSW3	C1	I	LVCMOS33	Rotary switch 3
DSW0	F5	I	LVCMOS33	DIP switch 0
DSW1	K7	I	LVCMOS33	DIP switch 1
DSW2	K8	I	LVCMOS33	DIP switch 2
DSW3	D5	I	LVCMOS33	DIP switch 3
DSW4	E4	I	LVCMOS33	DIP switch 4
DSW5	J7	I	LVCMOS33	DIP switch 5
DSW6	H8	I	LVCMOS33	DIP switch 6
DSW7	B2	I	LVCMOS33	DIP switch 7
LED0	G7	O	LVCMOS33	LED0
LED1	F7	O	LVCMOS33	LED1
LED2	D3	O	LVCMOS33	LED2
LED3	C4	O	LVCMOS33	LED3
LED4	E5	O	LVCMOS33	LED4
LED5	E6	O	LVCMOS33	LED5
LED6	A2	O	LVCMOS33	LED6
LED7	B3	O	LVCMOS33	LED7

Note: Input Video Status[1:0]

This status shows 2D / 3D video format.

[1:0] = “00” : 2D video.

[1:0] = “01” : 3D video. SideBySide format.

[1:0] = “10” : 3D video. TopAndBottom format.

[1:0] = “11” : 3D video. FramePacking format.

5.11. FPGA Input Data Phase

Figure 5-6 shows the input data phase of the FPGA on the TB-FMCH-HDMI2-TX.
FMC connector to FPGA data is captured by the FPGA at the rising edge of a video clock. Data from the main board is transferred at the falling edge of a video clock.

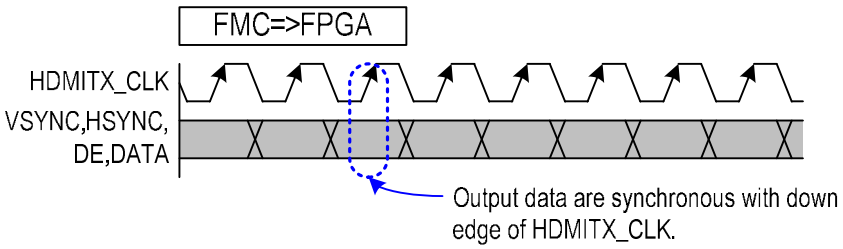

Figure 5-6 FPGA Input Data Timing

5.12. Audio(I2S format)

This design supports I2S format audio. Figure 5-7 shows audio output timing chart.
FPGA does not synchronaise audio signals to ADV7511.

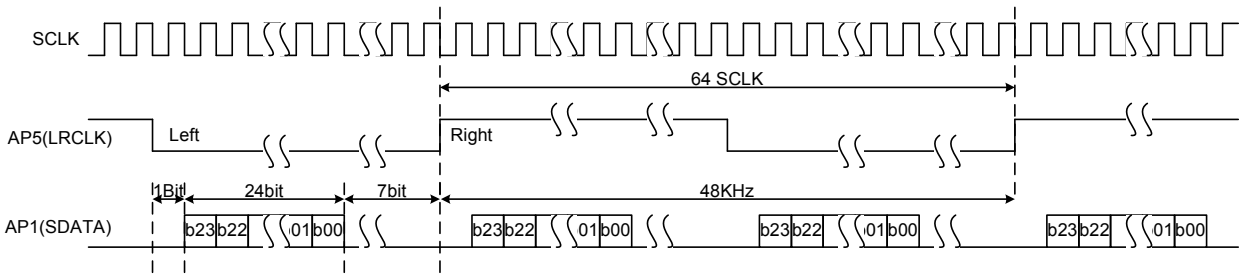

Figure 5-7 I2S Format Audio Timing Chart

5.13. Image Size

5.13.1. 2D Image Size

TB-FMCH-HDMI2-TX supports HDMI1.4-compliant primary format and part of secondary format (1080p@60Hz).

Supported image size:

- 640x480p@59.94/60Hz
- 1280x720p@59.94/60Hz
- 1920x1080i@59.94/60Hz
- 720x480p @ 59.94/60Hz
- 720(1440)x480i@59.94/60Hz
- 1280x720@50Hz
- 1920x1080i@50Hz
- 720x576p@50Hz
- 720(1440)x576i@50Hz
- 1920x1080p@59.94/60Hz
- 1920x1080p@50Hz

5.13.2. 3D Image Size

TB-FMCH-HDMI2-RX supports HDMI1.4-compliant primary format.

Supported image size:

- 1280x720p@59.94/60Hz (Frame Packing, Side-by-Side(Half), Top-and-Bottom)
- 1280x720p@50Hz (Frame Packing, Side-by-Side(Half), Top-and-Bottom)
- 1280x720p@23.98/24Hz (Frame Packing)
- 1280x720p@23.97/30Hz (Frame Packing)
- 1920x1080i@59.94/60Hz (Frame Packing, Side-by-Side(Half))
- 1920x1080i@50Hz (Frame Packing, Side-by-Side(Half))
- 1920x1080p@23.98/24Hz (Frame Packing, Side-by-Side(Half), Top-and-Bottom)
- 1920x1080p@29.97/30Hz (Frame Packing, Top-and-Bottom)
- 1920x1080p@59.94/60Hz (Top-and-Bottom)
- 1920x1080p@50Hz (Top-and-Bottom)

6. DDC Connection (Normal/ Through)

Two types of DDC connections are supported:

6.1. DDC Connection (Normal)

Table 6-1 shows DDC connection jumper setting (Normal) and Figure 6-1 shows DDC connection structure.

Table 6-1 DDC Jumper Setting (Normal)

TB-FMCH-HDMI2-RX		TB-FMCH-HDMI2-TX	
Jumper	Setting	Jumper	Setting
JP6: SCL0	1-2 short: Normal	-	-
JP7: SDA0	1-2 short: Normal	-	-
JP8: DDC0_5V	1-2 short: Normal	JP7: DDC0_5V	1-2 short: Normal
JP9: DDC0_HPD	1-2 short: Normal	JP8: DDC0_HPD	1-2 short: Normal
JP10: DDC0_SDA	1-2 short: Normal	JP4: DDC0_SDA	1-2 short: Normal
JP11: DDC0_SCL	1-2 short: Normal	JP5: DDC0_SCL	1-2 short: Normal
JP12: DDC0_GND	1-2 short: Normal	JP6: DDC0_GND	1-2 short: Normal
JP3: SCL1	1-2 short: Normal	-	-
JP4: SDA1	1-2 short: Normal	-	-
JP13: DDC1_5V	1-2 short: Normal	JP12: DDC1_5V	1-2 short: Normal
JP14: DDC1_HPD	1-2 short: Normal	JP13: DDC1_HPD	1-2 short: Normal
JP15: DDC1_SDA	1-2 short: Normal	JP9: DDC1_SDA	1-2 short: Normal
JP16: DDC1_SCL	1-2 short: Normal	JP10: DDC1_SCL	1-2 short: Normal
JP17: DDC1_GND	1-2 short: Normal	JP11: DDC1_GND	1-2 short: Normal

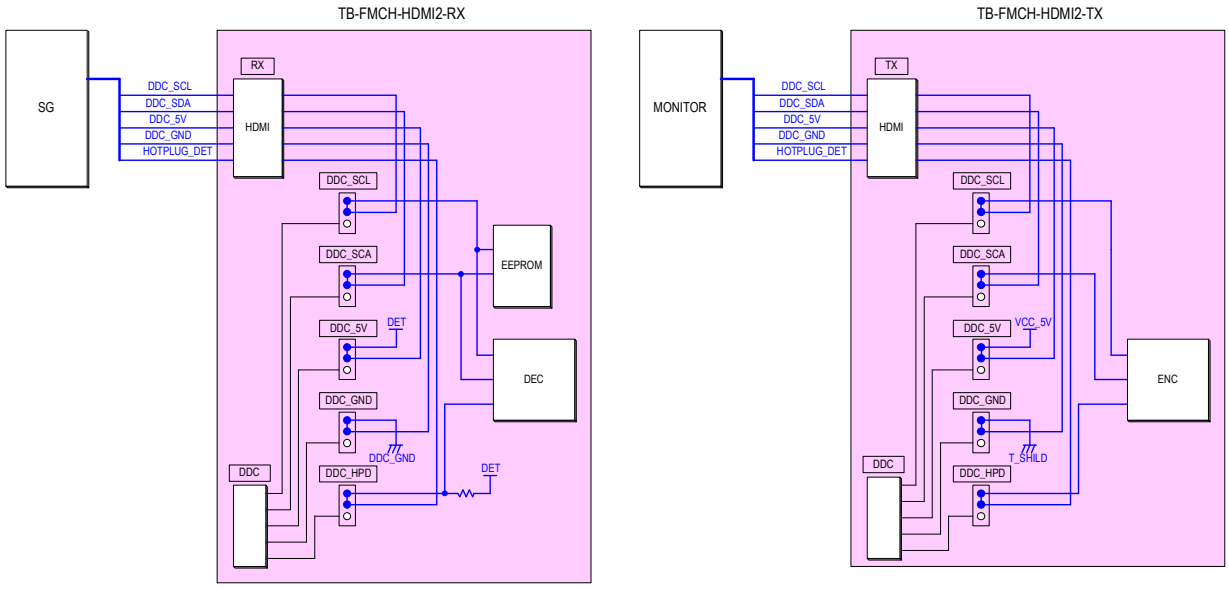

Figure 6-1 DDC Connection Structure (Normal)

6.2. DDC Connection (Through)

Table 6-2 shows DDC connection jumper setting (Through) and Figure 6-2 shows DDC connection structure (Through).

Table 6-2 DDC Jumper Setting (Through)

TB-FMCH-HDMI2-RX		TB-FMCH-HDMI2-TX	
Jumper	Setting	Jumper	Setting
JP6: SCL0	Open	-	-
JP7: SDA0	Open	-	-
JP8: DDC0_5V	1-2 short: Normal	JP7: DDC0_5V	1-2 short: Normal
JP9: DDC0_HPD	1-2 short: Normal	JP8: DDC0_HPD	1-2 short: Normal
JP10: DDC0_SDA	2-3 short: Through	JP4: DDC0_SDA	2-3 short: Through
JP11: DDC0_SCL	2-3 short: Through	JP5: DDC0_SCL	2-3 short: Through
JP12: DDC0_GND	2-3 short: Through	JP6: DDC0_GND	2-3 short: Through
JP3: SCL1	Open	-	-
JP4: SDA1	Open	-	-
JP13: DDC1_5V	1-2 short: Normal	JP12: DDC1_5V	1-2 short: Normal
JP14: DDC1_HPD	1-2 short: Normal	JP13: DDC1_HPD	1-2 short: Normal
JP15: DDC1_SDA	2-3 short: Through	JP9: DDC1_SDA	2-3 short: Through
JP16: DDC1_SCL	2-3 short: Through	JP10: DDC1_SCL	2-3 short: Through
JP17: DDC1_GND	2-3 short: Through	JP11: DDC1_GND	2-3 short: Through

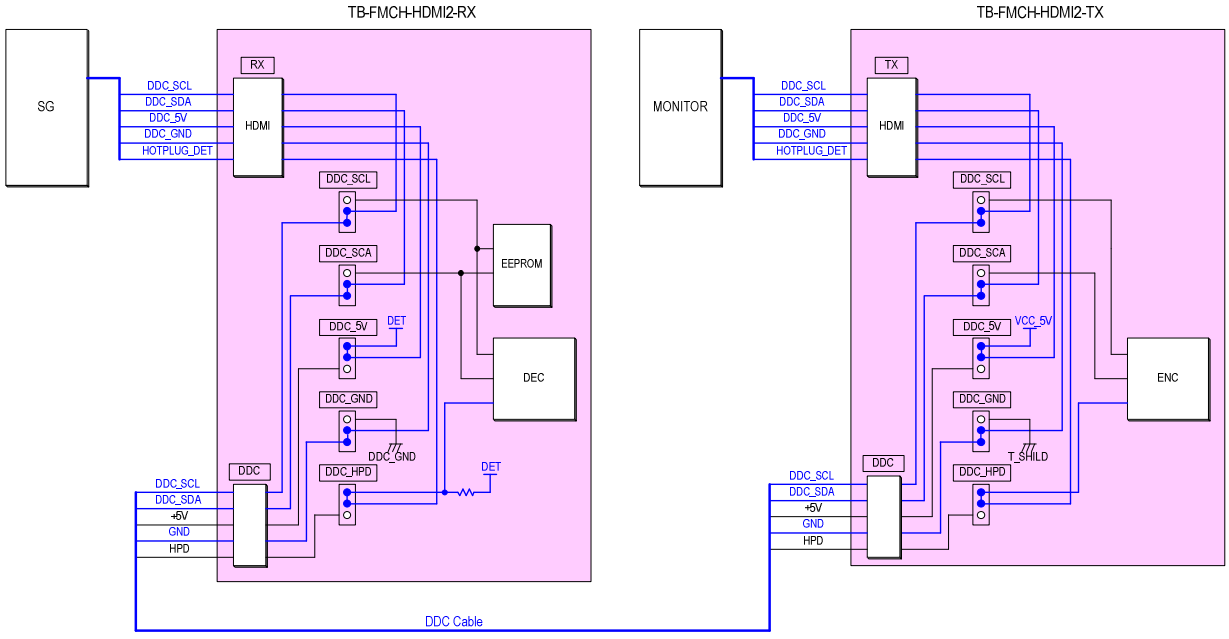

Figure 6-2 DDC Connection Structure (Through)

*To select DDC connection (Through), connect RX board-J4 and TX board -J1 or RX board-J2 and TX board -J3 using an attached cable.

7. Default Switch Setting

Figure 7-1 shows default TB-FMCH-HDMI2-RX switch settings (portions enclosed by dotted lines).

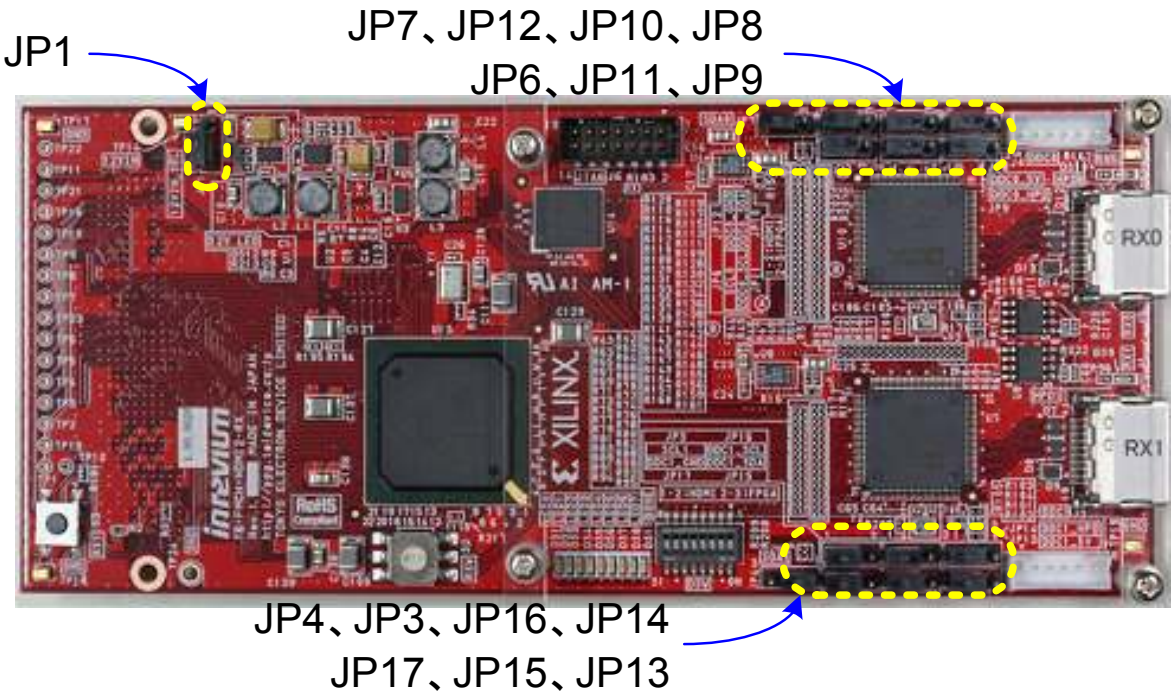

Figure 7-1 TB-FMCH-HDMI2-RX Default Switch Settings (component side)

Table 7-1 TB-FMCH-HDMI2-RX Default Settings (JP pin)

No.	Silk No.	Initial Setting	Function
1	JP6	1-2 short	SCL0 (1-2: HDMI / 2-3: FPGA)
2	JP7	1-2 short	SDA0 (1-2: HDMI / 2-3: FPGA)
3	JP8	1-2 short	DDC0_5V (1-2: Normal / 2-3: Through)
4	JP9	1-2 short	DDC0_HPD (1-2: Normal / 2-3: Through)
5	JP10	1-2 short	DDC0_SDA (1-2: Normal / 2-3: Through)
6	JP11	1-2 short	DDC0_SCL (1-2: Normal / 2-3: Through)
7	JP12	1-2 short	DDC0_GND (1-2: Normal / 2-3: Through)
8	JP3	1-2 short	SCL1 (1-2: HDMI / 2-3: FPGA)
9	JP4	1-2 short	SDA1 (1-2: HDMI / 2-3: FPGA)
10	JP13	1-2 short	DDC1_5V (1-2: Normal / 2-3: Through)
11	JP14	1-2 short	DDC1_HPD (1-2: Normal / 2-3: Through)
12	JP15	1-2 short	DDC1_SDA (1-2: Normal / 2-3: Through)
13	JP16	1-2 short	DDC1_SCL (1-2: Normal / 2-3: Through)
14	JP17	1-2 short	DDC1_GND (1-2: Normal / 2-3: Through)
15	JP1	1-2 short	12VIN_SEL (1-2: FMC connector / 2-3: External power source)

Table 7-2 TB-FMCH-HDMI2-RX Default Setting (DSW/RSW)

No.	Silk No.	Default Setting	Function
1	S1-1	OFF	ADV7612 config ROM selection *Please refer to Table 4-8.
2	S1-2	OFF	
3	S1-3	OFF	
4	S1-4	OFF	
5	S1-5	OFF	Unused. Please set ON
6	S1-6	OFF	Unused. Please set ON
7	S1-7	OFF	Unused. Please set ON
8	S1-8	OFF	Unused. Please set ON
9	S2	0	Unused. Please set ‘0’

Figure 7-2 shows TB-FMCH-HDMI2-TX default switch settings (portions enclosed by dotted lines).

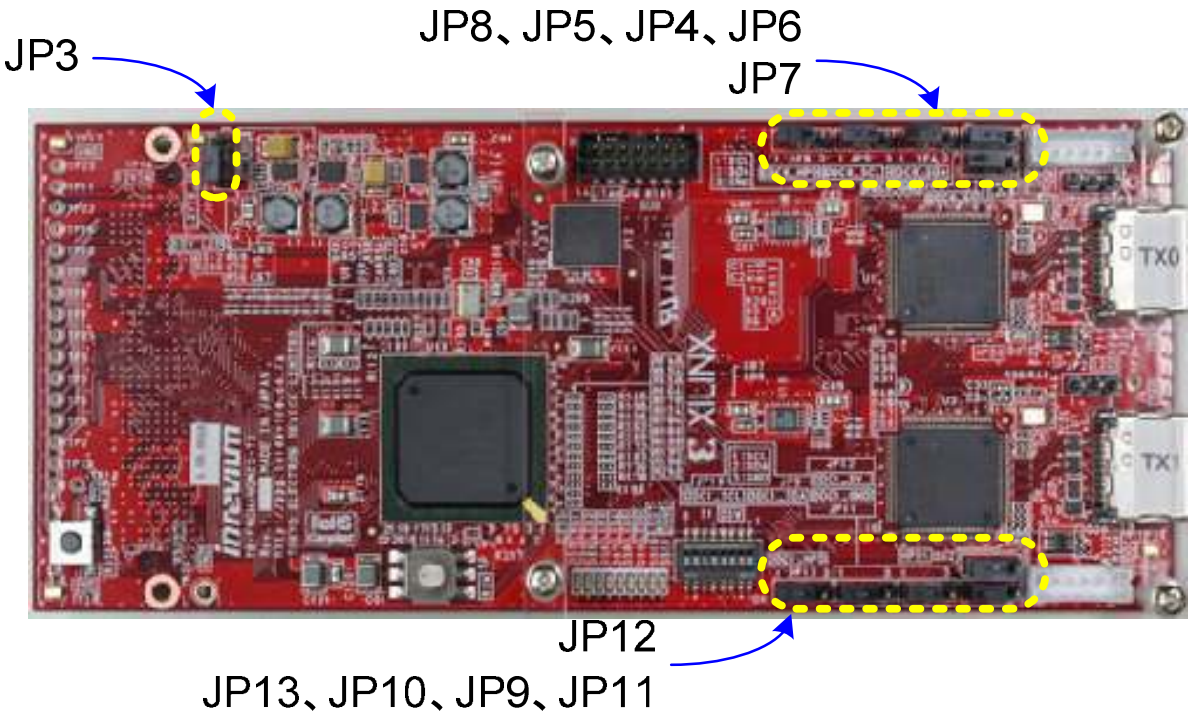

Figure 7-2 TB-FMCH-HDMI2-TX Default Settings (component side)

Table 7-3 TB-FMCH2-TX Default Settings (JP Pin)

No.	Silk No.	Initial Setting	Function
1	JP7	1-2 short	DDC0_5V (1-2: Normal / 2-3: Through)
2	JP8	1-2 short	DDC0_HPD (1-2: Normal / 2-3: Through)
3	JP4	1-2 short	DDC0_SDA (1-2: Normal / 2-3: Through)
4	JP5	1-2 short	DDC0_SCL (1-2: Normal / 2-3: Through)
5	JP6	1-2 short	DDC0_GND (1-2: Normal / 2-3: Through)
6	JP12	1-2 short	DDC1_5V (1-2: Normal / 2-3: Through)
7	JP13	1-2 short	DDC1_HPD (1-2: Normal / 2-3: Through)
8	JP9	1-2 short	DDC1_SDA (1-2: Normal / 2-3: Through)
9	JP10	1-2 short	DDC1_SCL (1-2: Normal / 2-3: Through)
10	JP11	1-2 short	DDC1_GND (1-2: Normal / 2-3: Through)
11	JP3	1-2 short	12VIN_SEL (1-2: FMC connector / 2-3: External power source)

Table 7-4 TB-FMCH-HDMI2-TX Default Switch Settings (DSW/RSW)

No.	Silk No.	Default Setting	Function
1	S1-1	OFF	ADV7511 config ROM selection: *Please see Table 5-7.
2	S1-2	OFF	
3	S1-3	OFF	
4	S1-4	OFF	
5	S1-5	OFF	Unused *set to ON.
6	S1-6	OFF	Unused *set to ON.
7	S1-7	OFF	Unused *set to ON.
8	S1-8	OFF	Unused *set to ON.
9	S2	0	Unused *set to '0'.

8. Usage Example

Figure 8-1 shows a usage example.
Be careful about the jumper setting of the TB-6S-LX150T-IMG2 main board.

If the image is not output, push the S3 of the TB-FMCH-HDMI2-RX or TB-FMCH-HDMI2-TX for only a short period of time.

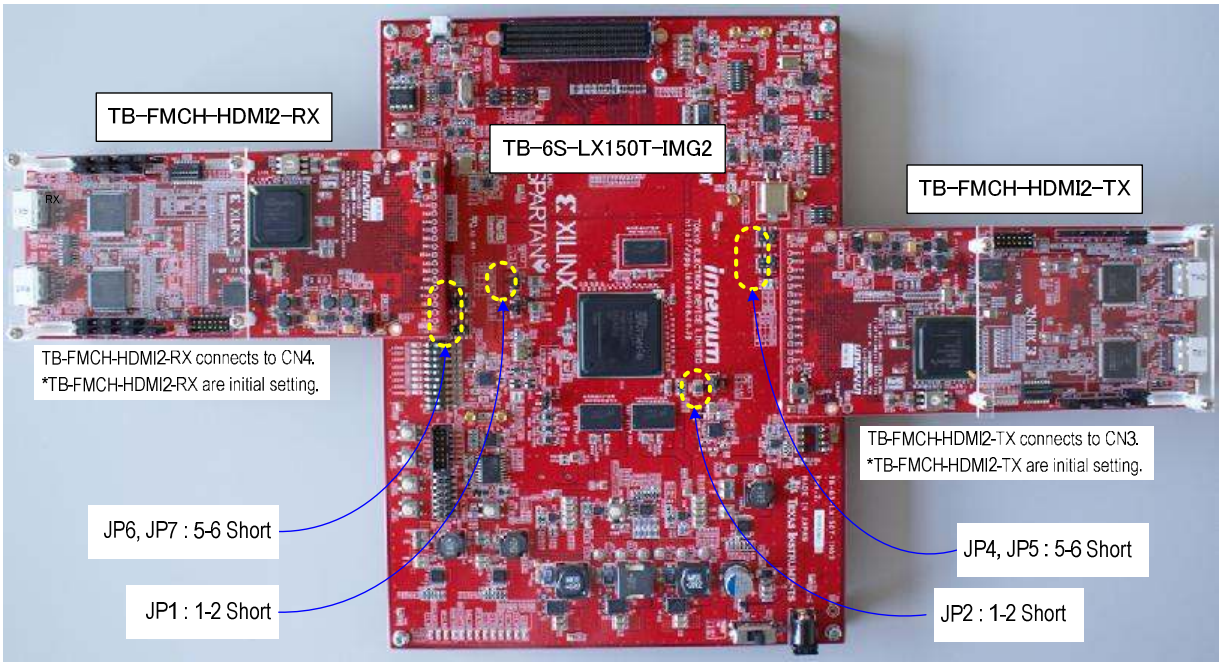

Figure 8-1 Usage Example

Table 8-1 Setting Example

No.	Silk No.	Setting	Function
1	JP1	1-2	Bank3 voltage setting (**2.5V** / 3.3V)
2	JP6 JP7	5-6	FMC-LPC2VADJ voltage setting (2.5V / 3.3V / **none**) (Two jumpers must be always the same)
3	JP2	1-2	Bank0 voltage setting (**2.5V** / 3.3V)
4	JP4 JP5	5-6	FMC-LPC1 VADJ voltage setting (2.5V / 3.3V /**none**) (Two jumpers must be always the same)

Note: The bold characters are the setting in the usage example.

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